

Electronic Design Automation Market Forecasts to 2034 – Global Analysis By Product (Computer-Aided Engineering (CAE), IC Physical Design & Verification, Printed Circuit Board (PCB) Design, Semiconductor IP (SIP), Multi-Chip Module (MCM) Design, and Other EDA Products), Deployment Mode, Design Type, Design Stage, Application, End User, and By Geography

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Abstracts

According to Statistics MRC, the Global Electronic Design Automation Market is accounted for \$22.6 billion in 2026 and is expected to reach \$54.5 billion by 2034 growing at a CAGR of 11.6% during the forecast period. Electronic Design Automation (EDA) refers to the software tools and services used for designing, simulating, verifying, and manufacturing electronic systems, including integrated circuits, printed circuit boards, systems-on-chip, field-programmable gate arrays, and electronic systems. These tools support the entire design lifecycle across system-level design, front-end design, back-end design, design verification, and manufacturing sign-off stages. The market serves semiconductor companies, electronics manufacturers, fabless design houses, and research institutions. Growing complexity of semiconductor designs, increasing adoption of advanced process nodes, rising demand for AI and high-performance computing chips, and expanding electronics content across industries are key drivers of market expansion across all regions.

Market Dynamics:

Driver:

Increasing complexity of semiconductor and electronic designs

The growing complexity of semiconductor devices and electronic systems is a primary driver for the EDA market. Advanced process nodes below 5nm, heterogeneous integration, and complex chiplet architectures require sophisticated design and verification tools that can handle billions of transistors and intricate interconnections. The shift toward domain-specific architectures for AI, automotive, and high-performance computing applications creates demand for specialized design flows. System-level design requirements are expanding as electronic systems integrate multiple functions and domains. As design complexity continues increasing with each technology generation, demand for advanced EDA tools and services grows, sustaining strong market expansion across all application areas.

Restraint:

High licensing costs and consolidation in the EDA industry

The significant costs of EDA tool licenses and the concentrated market structure dominated by major vendors represent a major restraint for the market. Comprehensive EDA design flows require substantial investment in tool licenses, maintenance, and support. Smaller companies and startups may struggle to afford full suites of advanced tools. The consolidation of the EDA industry reduces competition and may limit pricing flexibility. Tool adoption creates dependency on specific vendors, affecting flexibility and negotiating power. These cost and industry structure factors may limit EDA adoption, particularly among emerging companies and in cost-sensitive regions.

Opportunity:

Integration of AI and machine learning in design flows

The growing integration of artificial intelligence and machine learning into EDA tools presents significant opportunities for market expansion. AI-powered design tools enable automated optimization, improved design quality, and reduced time-to-market. Machine learning algorithms assist in routing, placement, timing analysis, and design space exploration. AI-assisted verification accelerates simulation and reduces debugging time. Generative AI for RTL code generation and documentation is emerging. As AI capabilities advance and EDA vendors incorporate intelligent features, productivity improvements and new capabilities capture growing market share, enabling enhanced

design efficiency and performance.

Threat:

Competition from open-source and in-house tools

The increasing availability of open-source EDA tools and development of in-house design automation solutions poses significant threats to the commercial EDA market. Open-source tools including OpenROAD, Yosys, and various verification frameworks offer free alternatives for certain design tasks. Large semiconductor companies develop proprietary tools for specialized applications. Emerging companies may choose open-source solutions to reduce costs. This competition may limit market growth in certain segments and pressure commercial vendors to demonstrate value through advanced capabilities and productivity gains.

Covid-19 Impact:

The COVID-19 pandemic had a significant impact on the EDA market. Initial disruptions included reduced customer engagement, project delays, and supply chain challenges. However, the pandemic accelerated demand for semiconductors across consumer electronics, computing, and telecommunications. Semiconductor companies maintained EDA investment to support product development and technology roadmaps. Remote work accelerated adoption of cloud-based EDA solutions. Post-pandemic, semiconductor demand and design activity have remained strong, with continued investment in EDA tools for advanced node development and new chip architectures. The crisis reinforced the strategic importance of electronic design capabilities.

The Design Verification segment is expected to be the largest during the forecast period

The Design Verification segment is expected to account for the largest market share during the forecast period, driven by the increasing complexity of semiconductor designs and the growing need for comprehensive verification to ensure functional correctness and reliability. Design verification consumes a substantial portion of the overall design effort, with verification teams often outnumbering design teams for complex chips. The segment includes simulation, formal verification, emulation, and prototyping tools essential for identifying design errors before manufacturing. Growing complexity of AI chips, automotive electronics, and safety-critical applications intensifies verification requirements. As designs become more complex and quality standards rise, design verification maintains the largest design stage market share.

The System-on-Chip (SoC) Design segment is expected to have the highest CAGR during the forecast period

Over the forecast period, the System-on-Chip (SoC) Design segment is predicted to witness the highest growth rate, fueled by the increasing integration of multiple functions onto single chips for smartphones, automotive electronics, AI accelerators, and IoT devices. SoC designs combine processors, memory, accelerators, and peripherals, requiring comprehensive EDA tools across design, verification, and manufacturing sign-off stages. The segment benefits from growing demand for specialized SoCs for AI, automotive, and edge computing applications. Increasing SoC complexity drives demand for advanced design, verification, and implementation tools. As SoC adoption expands across applications, this segment delivers the fastest application growth.

Region with largest share:

During the forecast period, the North America region is expected to hold the largest market share, supported by the presence of major EDA vendors, strong semiconductor design activity, and significant technology investment. The United States leads regional growth with substantial EDA vendor presence and major semiconductor companies. Strong technology ecosystem including research universities and innovation centers drives continuous advancement. High investment in chip design for AI, data center, and automotive applications. With established vendor presence and significant design investment, North America maintains its dominant market position.

Region with highest CAGR:

Over the forecast period, the Asia-Pacific region is anticipated to exhibit the highest CAGR, driven by rapid semiconductor design expansion, growing chip design activity in China and India, and increasing fabless semiconductor companies. The region's large and growing electronics manufacturing base creates demand for EDA tools. China's investment in domestic semiconductor design and manufacturing supports market growth. India's expanding chip design services sector creates EDA demand. Government initiatives promoting domestic chip development are accelerating adoption. As semiconductor design activity expands across the region, Asia Pacific delivers the fastest EDA market growth globally.

Key players in the market

Some of the key players in Electronic Design Automation include Synopsys, Inc., Cadence Design Systems, Inc., Siemens Digital Industries Software, ANSYS, Inc., Keysight Technologies, Inc., Altium Limited, Zuken Inc., Silvaco Group, Inc., Empyrean Technology Co., Ltd., Aldec, Inc., Primarius Technologies Co., Ltd., eInfochips (Arrow Electronics), Dassault Systèmes SE, Xpeedic Technology Co., Ltd., and EasyEDA Technology Co., Ltd.

Key Developments:

In April 2026, Siemens announced an expanded collaboration with TSMC at the 2026 Technology Symposium to deliver AI-driven EDA automation, including automated Design Rule Check (DRC) fixes using its Fuse™ EDA AI System and Solido Simulation certification across TSMC's advanced A14 and N2P nodes.

In February 2026, Cadence completed the integration of its acquisition of Hexagon's Design & Engineering software business, expanding its capabilities into Physical AI, multi-body dynamics, and complex electromechanical design analysis.

In January 2026, Synopsys advanced its agentic AI strategy by expanding its Synopsys.ai full-stack EDA suite, enabling autonomous multi-die multi-physics optimization and automated physical verification for sub-2nm designs.

Products Covered:

Computer-Aided Engineering (CAE)

IC Physical Design and Verification

Printed Circuit Board (PCB) Design

Semiconductor IP (SIP)

Multi-Chip Module (MCM) Design

Other EDA Products

Deployment Modes Covered:

On-Premises

Cloud-Based

Hybrid Deployment

Design Types Covered:

Analog Design

Digital Design

Mixed-Signal Design

RF Design

Photonic Design

Design Stages Covered:

System-Level Design

Front-End Design

Back-End Design

Design Verification

Manufacturing Sign-Off

Applications Covered:

Integrated Circuit (IC) Design

Printed Circuit Board (PCB) Design

System-on-Chip (SoC) Design

FPGA Design

Electronic Systems Design

End Users Covered:

Semiconductor Companies

Fabless IC Companies

Integrated Device Manufacturers (IDMs)

Foundries

Electronics Manufacturing Services (EMS) Providers

Automotive Electronics Manufacturers

Aerospace and Defense Organizations

Consumer Electronics Companies

Telecommunications Equipment Manufacturers

Research Institutes and Universities

Regions Covered:

North America

United States

Canada

Mexico

Europe

United Kingdom

Germany

France

Italy

Spain

Netherlands

Belgium

Sweden

Switzerland

Poland

Rest of Europe

Asia Pacific

China

Japan

India

South Korea

Australia

Indonesia

Thailand

Malaysia

Singapore

Vietnam

Rest of Asia Pacific

South America

Brazil

Argentina

Colombia

Chile

Peru

Rest of South America

Rest of the World (RoW)

Middle East

Saudi Arabia

United Arab Emirates

Qatar

Israel

Rest of Middle East

Africa

South Africa

Egypt

Morocco

Rest of Africa

What our report offers:

Market share assessments for the regional and country-level segments

Strategic recommendations for the new entrants

Covers Market data for the years 2023, 2024, 2025, 2026, 2027, 2028, 2030, 2032 and 2034

Market Trends (Drivers, Constraints, Opportunities, Threats, Challenges, Investment Opportunities, and recommendations)

Strategic recommendations in key business segments based on the market estimations

Competitive landscaping mapping the key common trends

Company profiling with detailed strategies, financials, and recent developments

Supply chain trends mapping the latest technological advancements

Free Customization Offerings:

All the customers of this report will be entitled to receive one of the following free customization options:

Company Profiling

Comprehensive profiling of additional market players (up to 3)

SWOT Analysis of key players (up to 3)

Regional Segmentation

Market estimations, Forecasts and CAGR of any prominent country as per the client's interest (Note: Depends on feasibility check)

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