Fan-Out Wafer Level Packaging Market in US - Industry Outlook and Forecast 2020-2026

https://marketpublishers.com/r/F27CCD9AAC11EN.html
Date: April 2020
Pages: 92
Price: US$ 2,700.00 (Single User License)
ID: F27CCD9AAC11EN

Abstracts

The Fan-Out WLP technique involves cutting and separating the chip and then embedding the chip inside the panel. The procedure is to attach the chip face down to the Carrier, and the chip spacing should conform to the Pitch specification of the circuit design, while the receiver performs Molding to form a Panel. Follow-up will be separation, sealant panel and a vehicle for sealant panel Wafer shape, also called reconstruct Wafer (Reconstituted Wafer), can be widely used standard Wafer process, need is formed on the sealant panel circuit design. Since the area of the sealing panel is larger than that of the chip, not only can I/O contacts be made into the wafer area by Fan-In method; It can also be Fanned Out on a plastic mold to accommodate more I/O contacts.

This report contains market size and forecasts of Fan-Out Wafer Level Packaging in US, including the following market information:
US Fan-Out Wafer Level Packaging Market Revenue, 2015-2020, 2021-2026, ($ millions)
Top Five Competitors in US Fan-Out Wafer Level Packaging Market 2019 (%)
The global Fan-Out Wafer Level Packaging market was valued at 978 million in 2019 and is projected to reach US$ 1978.1 million by 2026, at a CAGR of 19.3% during the forecast period. While the Fan-Out Wafer Level Packaging market size in US was US$ XX million in 2019, and it is expected to reach US$ XX million by the end of 2026, with a CAGR of XX% during 2020-2026.

COVID-19 pandemic has big impact on Fan-Out Wafer Level Packaging businesses, with lots of challenges and uncertainty faced by many players of Fan-Out Wafer Level Packaging in US. This report also analyses and evaluates the COVID-19 impact on Fan-Out Wafer Level Packaging market size in 2020 and the next few years in US

Total Market by Segment:

US Fan-Out Wafer Level Packaging Market, By Type, 2015-2020, 2021-2026 ($ millions)
US Fan-Out Wafer Level Packaging Market Segment Percentages, By Type, 2019 (%)

High Density Fan-Out Package

Core Fan-Out Package

US Fan-Out Wafer Level Packaging Market, By Application, 2015-2020, 2021-2026 ($ millions)
US Fan-Out Wafer Level Packaging Market Segment Percentages, By Application, 2019 (%)

CMOS Image Sensor

A Wireless Connection

Logic and Memory Integrated Circuits

Mems and Sensors

Analog and Hybrid Integrated Circuits

Others

Competitor Analysis

The report also provides analysis of leading market participants including:
Total Fan-Out Wafer Level Packaging Market Competitors Revenues in US, by Players 2015-2020 (Estimated), ($ millions)
Total Fan-Out Wafer Level Packaging Market Competitors Revenues Share in US, by Players 2019 (%)

Further, the report presents profiles of competitors in the market, including the following:

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TSMC

ASE Technology Holding Co.

JCET Group

Amkor Technology

Siliconware Technology (SuZhou) Co.

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