

Fan-Out Wafer Level Packaging Market in Brazil - Industry Outlook and Forecast 2020-2026

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Abstracts

The Fan-Out WLP technique involves cutting and separating the chip and then embedding the chip inside the panel. The procedure is to attach the chip face down to the Carrier, and the chip spacing should conform to the Pitch specification of the circuit design, while the receiver performs Molding to form a Panel. Follow-up will be separation, sealant panel and a vehicle for sealant panel Wafer shape, also called reconstruct Wafer (Reconstituted Wafer), can be widely used standard Wafer process, need is formed on the sealant panel circuit design. Since the area of the sealing panel is larger than that of the chip, not only can I/O contacts be made into the wafer area by Fan-In method; It can also be Fanned Out on a plastic mold to accommodate more I/O contacts.

This report contains market size and forecasts of Fan-Out Wafer Level Packaging in Brazil, including the following market information:

Brazil Fan-Out Wafer Level Packaging Market Revenue, 2015-2020, 2021-2026, (\$ millions)

Top Five Competitors in Brazil Fan-Out Wafer Level Packaging Market 2019 (%)

The global Fan-Out Wafer Level Packaging market was valued at 978 million in 2019 and is projected to reach US\$ 1978.1 million by 2026, at a CAGR of 19.3% during the forecast period. While the Fan-Out Wafer Level Packaging market size in Brazil was US\$ XX million in 2019, and it is expected to reach US\$ XX million by the end of 2026, with a CAGR of XX% during 2020-2026.

COVID-19 pandemic has big impact on Fan-Out Wafer Level Packaging businesses, with lots of challenges and uncertainty faced by many players of Fan-Out Wafer Level Packaging in Brazil. This report also analyses and evaluates the COVID-19 impact on Fan-Out Wafer Level Packaging market size in 2020 and the next few years in Brazil

Total Market by Segment:

Brazil Fan-Out Wafer Level Packaging Market, By Type, 2015-2020, 2021-2026 (\$ millions)

Brazil Fan-Out Wafer Level Packaging Market Segment Percentages, By Type, 2019 (%)

High Density Fan-Out Package

Core Fan-Out Package

Brazil Fan-Out Wafer Level Packaging Market, By Application, 2015-2020, 2021-2026 (\$ millions)

Brazil Fan-Out Wafer Level Packaging Market Segment Percentages, By Application, 2019 (%)

CMOS Image Sensor

A Wireless Connection

Logic and Memory Integrated Circuits

Mems and Sensors

Analog and Hybrid Integrated Circuits

Others

Competitor Analysis

The report also provides analysis of leading market participants including:

Total Fan-Out Wafer Level Packaging Market Competitors Revenues in Brazil, by Players 2015-2020 (Estimated), (\$ millions)

Total Fan-Out Wafer Level Packaging Market Competitors Revenues Share in Brazil, by Players 2019 (%)

Further, the report presents profiles of competitors in the market, including the following:

TSMC

ASE Technology Holding Co.

JCET Group

Amkor Technology

Siliconware Technology (SuZhou) Co.

Contents

1 INTRODUCTION TO RESEARCH & ANALYSIS REPORTS

- 1.1 Fan-Out Wafer Level Packaging Market Definition
- 1.2 Market Segments
 - 1.2.1 Segment by Type
 - 1.2.2 Segment by Application
- 1.3 COVID-19 Impact: Brazil Fan-Out Wafer Level Packaging Market Overview
- 1.4 Features & Benefits of This Report
- 1.5 Methodology & Sources of Information
 - 1.5.1 Research Methodology
 - 1.5.2 Research Process
 - 1.5.3 Base Year
 - 1.5.4 Report Assumptions & Caveats

2 BRAZIL FAN-OUT WAFER LEVEL PACKAGING OVERALL MARKET SIZE

- 2.1 Brazil Fan-Out Wafer Level Packaging Market Size: 2020 VS 2026
- 2.2 Brazil Fan-Out Wafer Level Packaging Revenue, Prospects & Forecasts: 2015-2026

3 COMPANY LANDSCAPE

- 3.1 Top Fan-Out Wafer Level Packaging Players in Brazil (including Foreign and Local Companies)
- 3.2 Top Brazil Fan-Out Wafer Level Packaging Companies Ranked by Revenue
- 3.3 Brazil Fan-Out Wafer Level Packaging Revenue by Companies (including Foreign and Local Companies)
- 3.4 Top 3 and Top 5 Fan-Out Wafer Level Packaging Companies in Brazil, by Revenue in 2019
- 3.5 Brazil Manufacturers Fan-Out Wafer Level Packaging Product Type
- 3.6 Tier 1, Tier 2 and Tier 3 Fan-Out Wafer Level Packaging Players in Brazil
 - 3.6.1 List of Brazil Tier 1 Fan-Out Wafer Level Packaging Companies
 - 3.6.2 List of Brazil Tier 2 and Tier 3 Fan-Out Wafer Level Packaging Companies

4 SIGHTS BY PRODUCT

- 4.1 Overview
 - 4.1.1 By Type - Brazil Fan-Out Wafer Level Packaging Market Size Markets, 2020 &

2026

4.1.2 High Density Fan-Out Package

4.1.3 Core Fan-Out Package

4.2 By Type - Brazil Fan-Out Wafer Level Packaging Revenue & Forecasts

4.2.1 By Type - Brazil Fan-Out Wafer Level Packaging Revenue, 2015-2020

4.2.2 By Type - Brazil Fan-Out Wafer Level Packaging Revenue, 2021-2026

4.2.3 By Type - Brazil Fan-Out Wafer Level Packaging Revenue Market Share, 2015-2026

5 SIGHTS BY APPLICATION

5.1 Overview

5.1.1 By Application - Brazil Fan-Out Wafer Level Packaging Market Size, 2020 & 2026

5.1.2 CMOS Image Sensor

5.1.3 A Wireless Connection

5.1.4 Logic and Memory Integrated Circuits

5.1.5 Mems and Sensors

5.1.6 Analog and Hybrid Integrated Circuits

5.1.7 Others

5.2 By Application - Brazil Fan-Out Wafer Level Packaging Revenue & Forecasts

5.2.1 By Application - Brazil Fan-Out Wafer Level Packaging Revenue, 2015-2020

5.2.2 By Application - Brazil Fan-Out Wafer Level Packaging Revenue, 2021-2026

5.2.3 By Application - Brazil Fan-Out Wafer Level Packaging Revenue Market Share, 2015-2026

6 PLAYERS PROFILES

6.1 TSMC

6.1.1 TSMC Corporate Summary

6.1.2 TSMC Business Overview

6.1.3 TSMC Fan-Out Wafer Level Packaging Major Product Offerings

6.1.4 TSMC Revenue in Brazil (2015-2020)

6.1.5 TSMC Key News

6.2 ASE Technology Holding Co.

6.2.1 ASE Technology Holding Co. Corporate Summary

6.2.2 ASE Technology Holding Co. Business Overview

6.2.3 ASE Technology Holding Co. Fan-Out Wafer Level Packaging Major Product Offerings

6.2.4 ASE Technology Holding Co. Revenue in Brazil (2015-2020)

6.2.5 ASE Technology Holding Co. Key News

6.3 JCET Group

6.3.1 JCET Group Corporate Summary

6.3.2 JCET Group Business Overview

6.3.3 JCET Group Fan-Out Wafer Level Packaging Major Product Offerings

6.3.4 JCET Group Revenue in Brazil (2015-2020)

6.3.5 JCET Group Key News

6.4 Amkor Technology

6.4.1 Amkor Technology Corporate Summary

6.4.2 Amkor Technology Business Overview

6.4.3 Amkor Technology Fan-Out Wafer Level Packaging Major Product Offerings

6.4.4 Amkor Technology Revenue in Brazil (2015-2020)

6.4.5 Amkor Technology Key News

6.5 Siliconware Technology (SuZhou) Co.

6.5.1 Siliconware Technology (SuZhou) Co. Corporate Summary

6.5.2 Siliconware Technology (SuZhou) Co. Business Overview

6.5.3 Siliconware Technology (SuZhou) Co. Fan-Out Wafer Level Packaging Major Product Offerings

6.5.4 Siliconware Technology (SuZhou) Co. Revenue in Brazil (2015-2020)

6.5.5 Siliconware Technology (SuZhou) Co. Key News

6.6 Nepes

6.6.1 Nepes Corporate Summary

6.6.2 Nepes Business Overview

6.6.3 Nepes Fan-Out Wafer Level Packaging Major Product Offerings

6.6.4 Nepes Revenue in Brazil (2015-2020)

6.6.5 Nepes Key News

7 KEY MARKET TRENDS & INFLUENCES 2021-2026

7.1 PESTLE Analysis for Brazil Fan-Out Wafer Level Packaging Market

7.2 Market Opportunities & Trends

7.3 Market Drivers

7.4 Market Restraints

8 CONCLUSION

9 APPENDIX

- 9.1 Note
- 9.2 Examples of Clients
- 9.3 Disclaimer

List Of Tables

LIST OF TABLES

- Table 1. Key Players of Fan-Out Wafer Level Packaging in Brazil
- Table 2. Top Players in Brazil, Ranking by Revenue (2019)
- Table 3. Brazil Fan-Out Wafer Level Packaging Revenue by Companies, (US\$, Mn), 2015-2020
- Table 4. Brazil Fan-Out Wafer Level Packaging Revenue Share by Companies, 2015-2020
- Table 5. Brazil Fan-Out Wafer Level Packaging Sales by Companies, (K Units), 2015-2020
- Table 6. Brazil Fan-Out Wafer Level Packaging Sales Share by Companies, 2015-2020
- Table 7. Key Manufacturers Fan-Out Wafer Level Packaging Price (2015-2020) (US\$/Unit)
- Table 8. Brazil Manufacturers Fan-Out Wafer Level Packaging Product Type
- Table 9. List of Brazil Tier 1 Fan-Out Wafer Level Packaging Companies, Revenue (US\$, Mn) in 2019 and Market Share
- Table 10. List of Brazil Tier 2 and Tier 3 Fan-Out Wafer Level Packaging Companies, Revenue (US\$, Mn) in 2019 and Market Share
- Table 11. By Type - Fan-Out Wafer Level Packaging Revenue in Brazil (US\$, Mn), 2015-2020
- Table 12. By Type - Fan-Out Wafer Level Packaging Revenue in Brazil (US\$, Mn), 2021-2026
- Table 13. By Type - Fan-Out Wafer Level Packaging Sales in Brazil (K Units), 2015-2020
- Table 14. By Type - Fan-Out Wafer Level Packaging Sales in Brazil (K Units), 2021-2026
- Table 15. By Application - Fan-Out Wafer Level Packaging Revenue in Brazil, (US\$, Mn), 2015-2020
- Table 16. By Application - Fan-Out Wafer Level Packaging Revenue in Brazil, (US\$, Mn), 2021-2026
- Table 17. By Application - Fan-Out Wafer Level Packaging Sales in Brazil, (K Units), 2015-2020
- Table 18. By Application - Fan-Out Wafer Level Packaging Sales in Brazil, (K Units), 2021-2026
- Table 19. TSMC Corporate Summary
- Table 20. TSMC Fan-Out Wafer Level Packaging Product Offerings
- Table 21. TSMC Fan-Out Wafer Level Packaging Revenue (US\$, Mn), (2015-2020)

Table 22. ASE Technology Holding Co. Corporate Summary

Table 23. ASE Technology Holding Co. Fan-Out Wafer Level Packaging Product Offerings

Table 24. ASE Technology Holding Co. Fan-Out Wafer Level Packaging Revenue (US\$, Mn), (2015-2020)

Table 25. JCET Group Corporate Summary

Table 26. JCET Group Fan-Out Wafer Level Packaging Product Offerings

Table 27. JCET Group Fan-Out Wafer Level Packaging Revenue (US\$, Mn), (2015-2020)

Table 28. Amkor Technology Corporate Summary

Table 29. Amkor Technology Fan-Out Wafer Level Packaging Product Offerings

Table 30. Amkor Technology Fan-Out Wafer Level Packaging Revenue (US\$, Mn), (2015-2020)

Table 31. Siliconware Technology (SuZhou) Co. Corporate Summary

Table 32. Siliconware Technology (SuZhou) Co. Fan-Out Wafer Level Packaging Product Offerings

Table 33. Siliconware Technology (SuZhou) Co. Fan-Out Wafer Level Packaging Revenue (US\$, Mn), (2015-2020)

Table 34. Nepes Corporate Summary

Table 35. Nepes Fan-Out Wafer Level Packaging Product Offerings

Table 36. Nepes Fan-Out Wafer Level Packaging Revenue (US\$, Mn), (2015-2020)

List Of Figures

LIST OF FIGURES

Figure 1. Fan-Out Wafer Level Packaging Segment by Type

Figure 2. Fan-Out Wafer Level Packaging Segment by Application

Figure 3. Brazil Fan-Out Wafer Level Packaging Market Overview: 2020

Figure 4. Key Caveats

Figure 5. Fan-Out Wafer Level Packaging Market Size in Brazil, (US\$, Mn): 2020 VS 2026

Figure 6. Brazil Fan-Out Wafer Level Packaging Revenue, 2015-2026 (US\$, Mn)

Figure 7. The Top 3 and 5 Players Market Share by Fan-Out Wafer Level Packaging Revenue in 2019

Figure 8. By Type - Brazil Fan-Out Wafer Level Packaging Incremental Growth, (US\$, Mn), 2015-2026

Figure 9. By Type - Brazil Fan-Out Wafer Level Packaging Market Share, 2015-2026

Figure 10. By Application - Fan-Out Wafer Level Packaging Revenue in Brazil (US\$, Mn), 2020 & 2026

Figure 11. By Application - Brazil Fan-Out Wafer Level Packaging Market Share, 2015-2026

Figure 12. PEST Analysis for Brazil Fan-Out Wafer Level Packaging Market in 2020

Figure 13. Fan-Out Wafer Level Packaging Market Opportunities & Trends in Brazil

Figure 14. Fan-Out Wafer Level Packaging Market Drivers in Brazil

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