

COVID-19 Outbreak-Global Wafer Level Packaging Industry Market Report-Development Trends, Threats, Opportunities and Competitive Landscape in 2020

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Abstracts

Wafer-Level Packaging (WLP) refers to the technology of packaging an integrated circuit at wafer level, instead of the traditional process of assembling the package of each individual unit after wafer dicing. WLP is essentially a true chip-scale packaging (CSP) technology, since the resulting package is practically of the same size as the die. Furthermore, wafer-level packaging paves the way for true integration of wafer fab, packaging, test, and burn-in at wafer level, for the ultimate streamlining of the manufacturing process undergone by a device from silicon start to customer shipment. The Wafer Level Packaging market revenue was xx.xx Million USD in 2019, and will reach xx.xx Million USD in 2025, with a CAGR of x.x% during 2020-2025.

Under COVID-19 outbreak globally, this report provides 360 degrees of analysis from supply chain, import and export control to regional government policy and future influence on the industry. Detailed analysis about market status (2015-2020), enterprise competition pattern, advantages and disadvantages of enterprise products, industry development trends (2020-2025), regional industrial layout characteristics and macroeconomic policies, industrial policy has also been included. From raw materials to end users of this industry are analyzed scientifically, the trends of product circulation and sales channel will be presented as well. Considering COVID-19, this report provides comprehensive and in-depth analysis on how the epidemic push this industry transformation and reform.

In COVID-19 outbreak, Chapter 2.2 of this report provides an analysis of the impact of COVID-19 on the global economy and the Wafer Level Packaging industry. Chapter 3.7 covers the analysis of the impact of COVID-19 from the perspective of the industry chain.

In addition, chapters 7-11 consider the impact of COVID-19 on the regional economy.

The Wafer Level Packaging market can be split based on product types, major applications, and important countries as follows:

Key players in the global Wafer Level Packaging market covered in Chapter 12:

Applied Materials, Inc.

ASML Holding N.V

Jiangsu Changjiang Electronics Technology Co. Ltd.

Amkor Technology, Inc.

Qualcomm Technologies, Inc.

Toshiba Corporation

Tokyo Electron Ltd.

Deca Technologies

Lam Research Corporation

Fujitsu

In Chapter 4 and 14.1, on the basis of types, the Wafer Level Packaging market from 2015 to 2025 is primarily split into:

Fan-in WLP

Fan-out WLP

In Chapter 5 and 14.2, on the basis of applications, the Wafer Level Packaging market from 2015 to 2025 covers:

Electronics

IT & Telecommunication

Industrial

Automotive

Geographically, the detailed analysis of consumption, revenue, market share and growth rate, historic and forecast (2015-2025) of the following regions are covered in Chapter 6, 7, 8, 9, 10, 11, 14:

North America (Covered in Chapter 7 and 14)

United States

Canada

Mexico

Europe (Covered in Chapter 8 and 14)

Germany

UK
France
Italy
Spain
Russia
Others
Asia-Pacific (Covered in Chapter 9 and 14)
China
Japan
South Korea
Australia
India
Southeast Asia
Others
Middle East and Africa (Covered in Chapter 10 and 14)
Saudi Arabia
UAE
Egypt
Nigeria
South Africa
Others
South America (Covered in Chapter 11 and 14)
Brazil
Argentina
Columbia
Chile
Others

Years considered for this report:

Historical Years: 2015-2019

Base Year: 2019

Estimated Year: 2020

Forecast Period: 2020-2025

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