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Global Wafer-Level Silicon Photonics Test System Market Growth (Status and Outlook) 2026-2032

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Abstracts

The global Wafer-Level Silicon Photonics Test System market size is predicted to grow from US$ 240 million in 2025 to US$ 1130 million in 2032; it is expected to grow at a CAGR of 22.6% from 2026 to 2032.

A Wafer-Level Silicon Photonics Test System is a dedicated wafer-level electro-optical test platform used to characterize, screen, and qualify silicon photonics devices, photonic integrated circuits, and related optoelectronic integrated chips before packaging. The scope of this study focuses on integrated test systems deployed at wafer, reticle, bar, or bare-die stages. A typical system combines a semi-automatic or fully automatic wafer prober, optical fiber or fiber-array coupling hardware, six-axis precision positioning and active optical alignment, electrical and RF probing, tunable lasers, optical power meters, polarization control, source-measure units, high-speed electrical instruments, temperature-controlled chucks, light-tight enclosures, machine vision, calibration algorithms, test automation software, data management, and factory automation interfaces. Its core functions include optical coupling, optical-electrical and electrical-optical measurement, passive photonic spectral characterization, active device LIV / EO / OE testing, RF and high-speed validation, process control monitoring, known-good-die identification, yield feedback, and production screening for silicon photonics foundries, IDMs, optical module makers, co-packaged optics suppliers, AI data-center optical interconnect manufacturers, and integrated photonics R&D platforms.

Based on our research, the wafer-level silicon photonics test system market should not be viewed as a simple extension of conventional electronic wafer probing. It is a cross-domain equipment segment that combines semiconductor test automation, precision optical coupling, electro-optical and RF measurement, active alignment, thermal control,

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calibration algorithms, and production data infrastructure. Conventional IC wafer test mainly focuses on electrical contact, pin count, parallelism, and parametric screening, while silicon photonics wafer test must also solve fiber-to-waveguide coupling, grating or edge-coupler alignment, polarization control, optical power stability, insertion loss repeatability, reflection effects, temperature drift, and high-speed optical-electrical correlation. For this reason, this study adopts a narrow revenue scope. General-purpose optical instruments, generic probers, packaged optical module testers, and testing services are not treated as core revenue unless they are delivered as part of a wafer-level silicon photonics test system. The broader supplier pool, however, still includes critical component suppliers and system integrators because the industry remains ecosystem-driven and project-based.

Demand is shifting from research labs and MPW characterization toward pilot production and early high-volume manufacturing. Before 2025, most demand came from silicon photonics foundries, IDMs, academic platforms, optical module companies, and early CPO programs. Starting in 2025?2026, AI data centers, 800G/1.6T optical interconnects, co-packaged optics, near-package optics, optical I/O, and hybrid-bonded PIC/EIC architectures are increasing the need for wafer-level screening. The economic driver is straightforward: once a photonic die is diced, assembled, fiber-attached, or co-packaged with electronic ICs, the cost of failure rises sharply. Wafer-level electro-optical screening therefore becomes a critical enabler of known-good-die selection, yield learning, process control, and cost reduction.

From a technology-roadmap perspective, three product families are likely to coexist. The first is flexible R&D and pilot-production PIC wafer or die test stations, which emphasize multi-device compatibility, rapid configuration, and support for both surface and edge coupling. The second is 200 mm and 300 mm automated wafer-level test systems for foundries and IDMs, which emphasize throughput, repeatability, thermal stability, factory automation, and traceable data. The third is high-volume double-sided electro-optical test cells and wafer-level burn-in or reliability systems for CPO, optical engines, and optical I/O devices. Edge coupling, grating coupling, wafer-level edge coupling, double-sided probing, fiber-array parallelism, RF-optical co-test, and automated calibration will become the key differentiators. The industry will remain customized in the near term, but the direction is clearly toward modularity, software-defined workflows, and open ecosystems that reduce integration burden for production customers.

From the competitive trend perspective, the silicon photonics wafer test system market is expected to move from customized engineering setups toward more standardized,

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production-ready test cells. In the early stage, many systems were assembled through a combination of a wafer prober, optical instruments, precision alignment stages, and customer-specific software. As silicon photonics, CPO, and optical I/O move closer to high-volume manufacturing, customers will increasingly require integrated platforms with higher throughput, better repeatability, automated optical alignment, double-sided probing capability, factory automation interfaces, and traceable production data. This transition favors vendors that can combine semiconductor ATE experience, photonics alignment expertise, optical-electrical measurement capability, and global service support. At the same time, regional suppliers, especially in China and Taiwan, are likely to gain share in engineering systems, pilot lines, and localized production support. Over the next few years, competition will not be determined only by instrument accuracy or prober performance, but by the ability to deliver a stable, scalable, and software-driven wafer-level test workflow. The market is therefore likely to evolve into a layered structure: a small group of global platform suppliers serving advanced HVM customers, several specialized photonics automation and probe-system vendors serving both R&D and production customers, and a broader group of regional integrators and component suppliers supporting localized applications.

LPI (LP Information)' newest research report, the ?Wafer-Level Silicon Photonics Test System Industry Forecast? looks at past sales and reviews total world Wafer-Level Silicon Photonics Test System sales in 2025, providing a comprehensive analysis by region and market sector of projected Wafer-Level Silicon Photonics Test System sales for 2026 through 2032. With Wafer-Level Silicon Photonics Test System sales broken down by region, market sector and sub-sector, this report provides a detailed analysis in US$ millions of the world Wafer-Level Silicon Photonics Test System industry.

This Insight Report provides a comprehensive analysis of the global Wafer-Level Silicon Photonics Test System landscape and highlights key trends related to product segmentation, company formation, revenue, and market share, latest development, and M&A activity. This report also analyses the strategies of leading global companies with a focus on Wafer-Level Silicon Photonics Test System portfolios and capabilities, market entry strategies, market positions, and geographic footprints, to better understand these firms? unique position in an accelerating global Wafer-Level Silicon Photonics Test System market.

This Insight Report evaluates the key market trends, drivers, and affecting factors shaping the global outlook for Wafer-Level Silicon Photonics Test System and breaks down the forecast by Type, by Application, geography, and market size to highlight emerging pockets of opportunity. With a transparent methodology based on hundreds of

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bottom-up qualitative and quantitative market inputs, this study forecast offers a highly nuanced view of the current state and future trajectory in the global Wafer-Level Silicon Photonics Test System.

This report presents a comprehensive overview, market shares, and growth opportunities of Wafer-Level Silicon Photonics Test System market by product type, application, key players and key regions and countries.

Segmentation by Type:

Integrated Wafer Test System

Other

Segmentation by Wafer / Device Format:

6-inch and Below Wafer Test

8-inch Wafer Test

12-inch Wafer Test

Other

Segmentation by Automation Level:

Manual Test System

Semi-Automated Test System

Fully Automated Wafer Test System

Segmentation by Measurement Configuration:

Optical-Only Configuration

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Electrical-Only Configuration

Optical-to-Electrical Configuration

Electrical-to-Optical Configuration

Other

Segmentation by Application:

R&D Characterization

Process Monitoring

Production Screening

Failure Analysis Support

Other

This report also splits the market by region:

Americas

United States

Canada

Mexico

Brazil

APAC

China

Japan

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- Korea
- Southeast Asia
- India
- Australia

Europe

- Germany
- France
- UK
- Italy
- Russia

Middle East & Africa

- Egypt
- South Africa
- Israel
- Turkey
- GCC Countries

The below companies that are profiled have been selected based on inputs gathered from primary experts and analyzing the company's coverage, product portfolio, its market penetration.

- Keysight Technologies, Inc.

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Teradyne, Inc.

FormFactor, Inc.

Advantest Corporation

Tokyo Electron Limited

MPI Corporation

RoboTechnik Intelligent Technology Co., Ltd.

EXFO Inc.

Semight Instruments Co., Ltd.

SEMISHARE CO., LTD.

STAr Technologies, Inc.

FIBERPRO, Inc.

SPEA S.p.A.

Aehr Test Systems

Enlitech

Yonata Electronics Co., Ltd.

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Contents

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3 WAFER-LEVEL SILICON PHOTONICS TEST SYSTEM MARKET SIZE BY PLAYER

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info@marketpublishers.com

+357 96 030922
info@marketpublishers.com

+357 96 030922
info@marketpublishers.com

9 MARKET DRIVERS, CHALLENGES AND TRENDS

10 GLOBAL WAFER-LEVEL SILICON PHOTONICS TEST SYSTEM MARKET FORECAST

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11 KEY PLAYERS ANALYSIS

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List Of Tables

LIST OF TABLES

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List Of Figures

LIST OF FIGURES

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