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Global Package Co-Design Software Market Growth (Status and Outlook) 2026-2032

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Abstracts

The global Package Co-Design Software market size is predicted to grow from US$ 895 million in 2025 to US$ 2242 million in 2032; it is expected to grow at a CAGR of 14.1% from 2026 to 2032.

Package Co-Design Software is a specialized electronic design automation software category for the coordinated development of semiconductor dies, chiplets, interposers, package substrates and, where required, printed circuit boards within a unified or tightly interoperable design environment. The market focuses on software that enables cross-domain architecture planning, die and chiplet placement, I/O and bump assignment, ball-map management, redistribution-layer and substrate routing, system connectivity management, physical verification and design closure. Depending on product architecture, these platforms may further integrate signal and power integrity, electromagnetic, thermal, mechanical stress and warpage analysis to support electrical and multiphysics optimization earlier in the design cycle. Major product forms include integrated co-design platforms, physical-design software, electrical-analysis software, multiphysics-analysis software and verification software. The principal technical scenarios include chip-package co-design, multi-die/package co-design, package-board co-design and chip-package-board co-design, serving advanced packaging architectures such as chiplets, 2.5D interposer systems, 3D stacked ICs, SiP and fan-out packages. The market is particularly relevant where package architecture materially affects system performance, power delivery, thermal behavior, interconnect density and reliability.

Key Findings

Commercial supply is concentrated in North America, Europe, China and Japan

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Integrated co-design platforms represent the largest value pool within the current product structure

Chiplet, 2.5D/3D IC and chip-package-board workflows are the primary technical deployment scenarios

AI and high-performance computing are the highest-priority application opportunities for advanced co-design tools

Market Trends

Package Co-Design Software is evolving from conventional package-layout automation toward system-level, multi-domain co-design. The most important product transition is the integration of architecture planning, physical implementation, electrical verification and multiphysics analysis into a more continuous workflow, allowing package constraints to influence chip and system decisions earlier. Chiplet-based architectures, HBM integration, high-speed die-to-die interfaces and 2.5D/3D stacking are increasing the need for cross-domain data consistency and automated design-space exploration. Foundry ecosystem validation is also becoming more important: TSMC’s 3DFabric EDA certification framework includes Chip / Package Co-Design among the certified design-solution categories for major EDA platforms, reinforcing the shift toward validated, system-level advanced-packaging flows.

Market Dynamics

Drivers

The primary growth driver is the increasing system complexity created by heterogeneous integration. AI accelerators, high-bandwidth memory, high-speed networking silicon and multi-die processors place tighter requirements on interconnect density, power delivery, thermal management and mechanical reliability, making sequential chip and package design less efficient. Broader EDA demand also remains supportive: SEMI’s ESD Alliance reported continued growth across all major electronic-design product categories in the first quarter of 2026, indicating sustained investment in design productivity and verification capability.

Restraints

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The principal market restraint is the high technical and ecosystem entry barrier. Commercially credible Package Co-Design Software requires accurate physical engines, scalable design databases, signoff-quality verification, process and packaging enablement, interoperability with adjacent EDA tools and substantial technical support. Enterprise licensing is also frequently bundled across broader EDA portfolios, making product-level purchasing decisions less transparent and raising switching costs for established customers. Smaller suppliers may therefore achieve technical differentiation in individual functions while facing longer qualification cycles in large semiconductor programs.

Opportunities

The strongest opportunities are emerging around chiplet system planning, automated multi-die physical implementation, electrical-thermal-mechanical co-optimization and AI-assisted design exploration. Package complexity is shifting engineering effort upstream, creating demand for tools that can evaluate interconnect, power, thermal and manufacturability constraints before detailed implementation. Additional opportunity exists in localized design ecosystems, particularly where domestic semiconductor companies seek alternative EDA supply, closer process support and faster customization for advanced packaging technologies.

Challenges

Long-term challenges include fragmented package design methodologies, differences among foundry and OSAT process environments, incomplete standardization of multi-die design data and the difficulty of correlating electrical, thermal and mechanical results at signoff accuracy. The market must also manage rapid technology transitions in interposers, hybrid bonding, high-density RDL and die-to-die interfaces. For emerging suppliers, technical credibility alone may be insufficient; commercial adoption depends heavily on reference customers, ecosystem certification, interoperability and long-term support capability.

Value Chain Analysis

The upstream layer of the Package Co-Design Software value chain consists primarily of semiconductor process and packaging design information, package and interface standards, EDA computational technologies, numerical solvers, high-performance computing resources and foundry/OSAT design-enablement infrastructure. Unlike manufacturing industries, the principal cost inputs are not physical materials but highly specialized engineering talent, algorithm development, software infrastructure,

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computing resources and continuous validation against evolving semiconductor and packaging technologies. Process design kits, package design kits, interface models and reference flows are critical inputs because they determine whether software can be used reliably in production-oriented design environments.

The midstream layer comprises Package Co-Design Software developers that convert these inputs into architecture-planning, physical-design, verification and multiphysics platforms and monetize them through licenses, subscriptions, enterprise agreements and technical services. Value creation is concentrated in solver accuracy, database scalability, automation, interoperability, ecosystem certification and workflow integration. Downstream value is realized by semiconductor design companies, integrated device manufacturers, system developers and advanced-packaging ecosystems that use these tools to shorten design iterations, reduce late-stage package rework and improve system-level performance, power and reliability.

Segment Insights

By product type, Integrated Co-Design Platforms form the largest value pool in the current study structure because leading platforms combine planning, physical implementation, connectivity management and multiple verification domains within a common environment. Physical Design Software remains an important category for package, RDL and interposer implementation, while Electrical Analysis Software and Multiphysics Analysis Software gain strategic importance as high-speed interfaces, HBM and dense 3D structures increase the interaction between electrical, thermal and mechanical constraints. Verification Software remains essential for physical consistency and system connectivity closure.

By technical deployment, Multi-Die–Package Co-Design and Chip–Package–Board Co-Design are among the most commercially significant directions. Chiplet and 2.5D/3D IC projects require larger design spaces, more interfaces and earlier package-aware optimization than conventional single-die packages. As a result, growth opportunities increasingly favor products that connect architecture planning with automated routing, SI/PI analysis, thermal and stress evaluation and final physical verification rather than stand-alone point tools.

Downstream Market Opportunities

AI & High-Performance Computing represents the highest-priority opportunity for Package Co-Design Software because advanced processors increasingly combine

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large logic dies, chiplets, HBM and high-density package interconnects under strict power and thermal constraints. Data Center & Networking is another important opportunity as high-speed SerDes and switch architectures raise package-level signal and power integrity requirements. Automotive Electronics and Telecommunications provide additional demand for high-reliability and RF/high-speed co-design, while Consumer Electronics and Industrial Electronics support broader adoption of SiP, fan-out and heterogeneous-integration workflows.

Regional Insights

North America is the most mature commercial market for Package Co-Design Software, supported by the concentration of major EDA platforms, advanced processor developers, cloud and AI system companies and a well-established semiconductor design ecosystem. As a directional benchmark for the broader electronic-design market, SEMI's ESD Alliance reported that the Americas remained the largest ESD purchasing region in the first quarter of 2026, while Asia-Pacific recorded 17.7% year-on-year growth, the strongest among the major reported regions.

Asia-Pacific represents the most important incremental opportunity because the region combines advanced packaging manufacturing, foundry and OSAT capacity, memory production and a rapidly expanding local EDA ecosystem. China is notable for the increasing number of domestic Package Co-Design Software suppliers, while Japan maintains specialized strength in chip-package-board and package-design software. South Korea and Taiwan are strategically important demand and ecosystem centers, although the confirmed independent commercial software-supplier base remains smaller than their advanced-packaging manufacturing footprint.

Competitive Landscape Analysis

The competitive structure of Package Co-Design Software is concentrated but increasingly differentiated by workflow depth. Cadence Design Systems, Synopsys and Siemens form the principal global integrated-platform group, supported by broad IC implementation, package design, physical verification and increasingly multiphysics capabilities; TSMC's current 3DFabric EDA certification framework provides additional validation of their role in advanced chip/package co-design. Keysight Technologies is differentiated in RF and high-speed multi-technology design, while Zuken has a distinct chip-package-board systems-design position. Monozukuri represents a specialized advanced-packaging co-design supplier, and the confirmed Chinese supplier group—Shanghai UniVista Industrial Software Group, Xpeedic, Shanghai Hongkuai

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Technology and BTD Technology—is expanding the regional competitive base through system-level connectivity, chiplet implementation, package-board collaboration and multiphysics workflows. Industry consolidation is also strengthening platform integration: Synopsys completed its acquisition of Ansys in July 2025 and stated that integrated multiphysics capabilities would extend across the EDA stack, including multi-die advanced packaging, while Siemens completed its acquisition of Altair in March 2025, adding further simulation, electromagnetic and engineering-analysis capabilities. These developments point toward competition based increasingly on full-flow integration, verified ecosystem compatibility and system-level optimization rather than isolated package-design functions.

Report Scope

LPI (LP Information)' newest research report, the “Package Co-Design Software Industry Forecast” looks at past sales and reviews total world Package Co-Design Software sales in 2025, providing a comprehensive analysis by region and market sector of projected Package Co-Design Software sales for 2026 through 2032. With Package Co-Design Software sales broken down by region, market sector and sub-sector, this report provides a detailed analysis in US$ millions of the world Package Co-Design Software industry.

This Insight Report provides a comprehensive analysis of the global Package Co-Design Software landscape and highlights key trends related to product segmentation, company formation, revenue, and market share, latest development, and M&A activity. This report also analyses the strategies of leading global companies with a focus on Package Co-Design Software portfolios and capabilities, market entry strategies, market positions, and geographic footprints, to better understand these firms’ unique position in an accelerating global Package Co-Design Software market.

This Insight Report evaluates the key market trends, drivers, and affecting factors shaping the global outlook for Package Co-Design Software and breaks down the forecast by Type, by Application, geography, and market size to highlight emerging pockets of opportunity. With a transparent methodology based on hundreds of bottom-up qualitative and quantitative market inputs, this study forecast offers a highly nuanced view of the current state and future trajectory in the global Package Co-Design Software.

This report presents a comprehensive overview, market shares, and growth opportunities of Package Co-Design Software market by product type, application, key

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players and key regions and countries.

Market Segmentation

Segmentation by Type:

Integrated Co-Design Platform

Electrical Analysis Software

Multiphysics Analysis Software

Other

Segmentation by Co-Design Scope:

Chip–Package Co-Design

Multi-Die–Package Co-Design

Package–Board Co-Design

Chip–Package–Board Co-Design

Segmentation by Packaging Architecture:

Organic Substrate Package

Silicon Interposer Package

3D Stacked Package

Other

Segmentation by High-Speed Interface Data Rate:

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?32 Gbps/lane Standard-Speed Design

>32–112 Gbps/lane High-Speed Design

>112 Gbps/lane Ultra-High-Speed Design

Segmentation by Application:

AI & High-Performance Computing

Data Center & Networking

Consumer Electronics

Aerospace & Defense

Medical Electronics

Other Applications

This report also splits the market by region:

Americas

United States

Canada

Mexico

Brazil

APAC

China

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- Japan
- Korea
- Southeast Asia
- India
- Australia

Europe

- Germany
- France
- UK
- Italy
- Russia

Middle East & Africa

- Egypt
- South Africa
- Israel
- Turkey
- GCC Countries

The below companies that are profiled have been selected based on inputs gathered from primary experts and analyzing the company's coverage, product portfolio, its market penetration.

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Siemens AG

Synopsys, Inc.

Cadence Design Systems, Inc.

Keysight Technologies, Inc.

Zuken Inc.

Shanghai UniVista Industrial Software Group Co., Ltd.

Xpeedic Co., Ltd.

Monozukuri S.p.A.

Shanghai Hongkuai Technology Co., Ltd.

BTD Technology

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