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Global Large-Model AI Accelerator Chips Market Growth 2026-2032

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Abstracts

The global Large-Model AI Accelerator Chips market size is predicted to grow from US$ 50615 million in 2025 to US$ 167418 million in 2032; it is expected to grow at a CAGR of 18.7% from 2026 to 2032.

In 2025, global Large-Model AI Accelerator Chips capacity 7,000 k Pcs, sales reached approximately 6,500 k Pcs, with an average market price of around 7,960 USD/Pcs, industrial gross margin 56%.

Large-Model AI Accelerator Chips are purpose-built processors optimized for the training, post-training and inference of large language models, multimodal foundation models, reasoning systems and increasingly agentic workloads. The category encompasses data-center GPUs, TPU/NPU-class ASICs, hyperscaler-designed XPUs and emerging LPU, RDU, wafer-scale and inference-specific architectures, while excluding general-purpose CPUs, standalone HBM, networking ASICs, optical modules and server systems themselves. The performance envelope has expanded rapidly: leading 2025–2026 data-center accelerators are generally implemented on roughly 2–5 nm process technologies, provide about 96–432 GB of HBM-class memory per device, and deliver approximately 2.9–23.3 TB/s of memory bandwidth. Peak FP8 capability now ranges from roughly one to more than twenty PFLOPS across representative high-end processors, while leading FP4-class implementations extend into the tens of PFLOPS. This makes memory capacity, realized bandwidth, interconnect performance, latency, token throughput and software efficiency as important as headline FLOPS.

The architecture landscape has evolved into a three-way contest among highly programmable GPUs, workload-optimized ASICs and dataflow or memory-centric designs, with data movement becoming the dominant system-level engineering

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problem. GPUs preserve maximum workload flexibility and benefit from mature programming ecosystems; hyperscaler ASICs such as TPU, Trainium, Maia and MTIA sacrifice some generality to optimize recurring internal workloads; and specialist vendors such as Cerebras, Groq, SambaNova and d-Matrix redesign compute around wafer-scale SRAM, deterministic execution, reconfigurable dataflow or in-memory processing. The semiconductor itself is only one layer of the competitive stack. Advanced logic nodes, HBM, 2.5D/3D packaging, chiplets, SerDes, board-level modules, scale-up fabrics, compilers, kernel libraries and distributed runtimes all determine realized model performance. At cluster scale, reliability, collective communication, model portability and software maturity become major barriers to entry.

Demand is broadening from episodic frontier-model pretraining into a persistent compute layer spanning reinforcement learning, synthetic-data generation, fine-tuning, online inference and autonomous-agent execution. Frontier laboratories emphasize low-precision training, HBM capacity, scale-up bandwidth and cluster utilization, whereas inference providers increasingly procure around time-to-first-token, inter-token latency, tokens per user, concurrency, KV-cache capacity and energy efficiency. Enterprise and sovereign deployments add requirements around security, virtualization, fault isolation, RAS and long-term software support. China has entered a second phase of domestic accelerator development in which basic model execution is no longer sufficient: rapid adaptation to DeepSeek, Qwen, GLM and other contemporary model families, support for frameworks such as vLLM and SGLang, high-bandwidth supernodes and large-cluster engineering have become core competitive criteria.

NVIDIA remains the benchmark platform because its accelerator roadmap is reinforced by CUDA, networking and rack-scale systems, but AMD, hyperscaler silicon and specialist inference architectures are creating credible workload-specific alternatives. NVIDIA Rubin combines 288 GB of HBM4 with 22 TB/s of bandwidth, while AMD's July 2026 MI455X increases device memory to 432 GB and bandwidth to 23.3 TB/s. Google Ironwood, AWS Trainium3 and Microsoft Maia 200 illustrate a second competitive axis in which hyperscalers vertically integrate silicon with their models, networks and data centers. Broadcom and Marvell occupy another structurally important position as custom-XPU development and implementation partners. A particularly significant development occurred on June 24, 2026, when OpenAI and Broadcom unveiled Jalape?o, OpenAI's first LLM-oriented Intelligence Processor. OpenAI defined the architecture around its inference workloads, Broadcom provided silicon implementation capabilities, and Celestica participated in board and rack industrialization, illustrating how model owners are increasingly influencing semiconductor architecture directly.

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The next competitive cycle will be driven less by isolated silicon benchmarks and more by the economics of heterogeneous AI factories. Reasoning models, long-context inference, multimodal generation and agentic workloads increase inference intensity and make prefill/decode disaggregation, heterogeneous acceleration and memory-aware scheduling increasingly attractive. Precision is moving from BF16 and FP8 toward FP4 and microscaled formats; HBM3E is transitioning to HBM4; chiplets, hybrid bonding, scale-up Ethernet/UALink and eventually co-packaged optics are expanding system bandwidth. At the same time, very-large-LPDDR, SRAM-centric and near-memory architectures are creating alternative inference designs. Commercial differentiation is consequently shifting toward rack-scale systems, compilers, inference engines, managed clouds and token services. The principal constraints remain software switching costs, advanced-packaging complexity, HBM availability, power and cooling infrastructure, cluster reliability, customer qualification cycles, geopolitical supply-chain restrictions and the risk that fixed-function silicon becomes misaligned with rapidly changing model architectures.

Report Scope

LP Information, Inc. (LPI) ' newest research report, the “Large-Model AI Accelerator Chips Industry Forecast” looks at past sales and reviews total world Large-Model AI Accelerator Chips sales in 2025, providing a comprehensive analysis by region and market sector of projected Large-Model AI Accelerator Chips sales for 2026 through 2032. With Large-Model AI Accelerator Chips sales broken down by region, market sector and sub-sector, this report provides a detailed analysis in US$ millions of the world Large-Model AI Accelerator Chips industry.

This Insight Report provides a comprehensive analysis of the global Large-Model AI Accelerator Chips landscape and highlights key trends related to product segmentation, company formation, revenue, and market share, latest development, and M&A activity. This report also analyzes the strategies of leading global companies with a focus on Large-Model AI Accelerator Chips portfolios and capabilities, market entry strategies, market positions, and geographic footprints, to better understand these firms’ unique position in an accelerating global Large-Model AI Accelerator Chips market.

This Insight Report evaluates the key market trends, drivers, and affecting factors shaping the global outlook for Large-Model AI Accelerator Chips and breaks down the forecast by Technical Architecture, by Application, geography, and market size to highlight emerging pockets of opportunity. With a transparent methodology based on hundreds of bottom-up qualitative and quantitative market inputs, this study forecast

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offers a highly nuanced view of the current state and future trajectory in the global Large-Model AI Accelerator Chips.

This report presents a comprehensive overview, market shares, and growth opportunities of Large-Model AI Accelerator Chips market by product type, application, key manufacturers and key regions and countries.

Market Segmentation

Segmentation by Technical Architecture:

GPU

FPGA

ASIC

Others

Segmentation by Function:

Training Chip

Inference Chip

Training & Inference Chip

Segmentation by Memory:

HBM-Centric

High-Capacity LPDDR

SRAM/Dataflow

Others

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Segmentation by Industry:

Data Center

Automobile

Robot

Consumer Electronics

Medical

Others

Segmentation by Application:

Cloud Server

Edge and Terminal (Mobile Device)

This report also splits the market by region:

Americas

United States

Canada

Mexico

Brazil

APAC

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China

Japan

Korea

Southeast Asia

India

Australia

Europe

Germany

France

UK

Italy

Russia

Middle East & Africa

Egypt

South Africa

Israel

Turkey

GCC Countries

The below companies that are profiled have been selected based on inputs gathered from primary experts and analysing the company's coverage, product portfolio, its

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market penetration.

NVIDIA

AMD

Intel

Google

Microsoft

Amazon

Samsung

Qualcomm

IBM

Apple

Meta

OpenAI/Broadcom

Cerebras Systems

Groq

Graphcore

Tenstorrent

Hailo

SambaNova

Huawei

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Cambricon

Horizon Robotics

Biren

Iluvatar CoreX

Moore Threads

MetaX

Enflame

Hygon Information Technology

Changsha Jingjia Microelectronics

Kunlunxin (Baidu)

T-Head (Alibaba)

Hexaflake

PostMoore Technology

SiEngine Technology

Key Questions Addressed in this Report

What is the 10-year outlook for the global Large-Model AI Accelerator Chips market?

What factors are driving Large-Model AI Accelerator Chips market growth, globally and by region?

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Which technologies are poised for the fastest growth by market and region?

How do Large-Model AI Accelerator Chips market opportunities vary by end market size?

How does Large-Model AI Accelerator Chips break out by Technical Architecture, by Application?

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