

Global Gearbox IC Market Growth 2026-2032

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Abstracts

The global Gearbox IC market size is predicted to grow from US\$ 386 million in 2025 to US\$ 1088 million in 2032; it is expected to grow at a CAGR of 15.8% from 2026 to 2032.

Gearbox chips are high-speed physical-layer connectivity ICs designed to establish stable data mapping and signal regeneration across different data rates, lane widths, modulation formats, and protocol generations. These devices typically integrate high-speed SerDes, CDR, equalization, lane remapping, rate conversion, forward error correction adaptation, diagnostic telemetry, and selected security functions, enabling differences between PAM4 and NRZ, high-speed single-lane and lower-speed multi-lane interfaces, new and legacy PCIe generations, and switch-chip-to-optical-module interfaces to be converted into deployable system links. Typical applications are concentrated in data center switches, AI cluster interconnects, 400G to 1.6T optical modules, active electrical cables, server board-level interconnects, carrier transport equipment, and high-end network line cards. As AI servers, cloud data centers, and high-speed Ethernet port density continue to increase, system designers face greater link loss, tighter power constraints, asynchronous protocol upgrades, and more complex board routing. Gearbox chips help equipment vendors extend link reach, improve port utilization, reduce system migration cost, and shorten the cycle from high-speed platform validation to mass production through protocol-transparent or protocol-aware high-speed physical-layer adaptation.

The industrial value of Gearbox ICs is increasing as data center interconnect architectures upgrade. Traditional high-speed interface chips mainly handled signal compensation and link extension, while new-generation products must perform more complex rate conversion and lane mapping among switch ASICs, optical modules, backplanes, line cards, and active electrical cables. As AI training and inference clusters expand, east-west traffic inside networks is growing rapidly, switch port rates are

moving from 400G to 800G, 1.6T, and 3.2T, and per-lane rates are advancing from 56G PAM4 to 112G and 212G PAM4. In this process, Gearbox ICs must not only solve interface compatibility across equipment generations, but also balance low power, low latency, low bit-error rate, and high signal integrity. Their positioning is shifting from auxiliary interface devices to critical link chips in high-speed network systems, especially in pluggable optical modules, AI backplane interconnects, switch line cards, and active electrical cables.

From a competitive perspective, Gearbox ICs depend heavily on high-speed SerDes, PAM4 DSP, equalization algorithms, low-jitter PLLs, advanced packaging, and system-level validation, creating high barriers to entry. Leading suppliers usually enter the market through PHY, DSP, or optical interconnect portfolios and improve platform reuse by supporting Retimer, Forward Gearbox, Reverse Gearbox, MUX, or security encryption functions in the same chip. Customers evaluate not only port rate and lane count, but also power consumption, latency, package size, reference design maturity, interoperability, and long-term supply capability. Because high-speed network equipment upgrade cycles are long, once a chip is designed into a switch, optical module, or line-card platform, it often has strong customer stickiness. Future competition will move from single-chip specifications toward complete interconnect solution capability, and suppliers with optical module, switch ASIC, high-speed copper cable, and AI network ecosystem resources are more likely to achieve large-scale adoption.

From a market outlook perspective, Gearbox ICs will benefit from AI infrastructure, high-speed Ethernet, cloud data centers, optical module upgrades, and telecom backbone expansion. AI clusters continue to raise requirements for bandwidth density and energy efficiency, driving ongoing iteration in switch ports, optical module speeds, and in-rack interconnect methods. At the same time, a large installed base of network equipment must maintain compatibility across interface generations, giving Forward Gearbox and Reverse Gearbox important bridging value during system upgrades. Although this market is smaller than the overall Ethernet PHY and optical DSP markets, it has high technical barriers, concentrated customers, and high product value density, resulting in strong growth elasticity. The Gearbox IC market is estimated at approximately 220 million usd in 2025 and 245 million usd in 2026, with an estimated CAGR of about 11.5% from 2026 to 2032. As 200G-per-lane, 3.2T PHY, 800G, and 1.6T optical module shipments expand, the industry still has room for sustained growth.

LP Information, Inc. (LPI) ' newest research report, the "Gearbox IC Industry Forecast" looks at past sales and reviews total world Gearbox IC sales in 2025, providing a

comprehensive analysis by region and market sector of projected Gearbox IC sales for 2026 through 2032. With Gearbox IC sales broken down by region, market sector and sub-sector, this report provides a detailed analysis in US\$ millions of the world Gearbox IC industry.

This Insight Report provides a comprehensive analysis of the global Gearbox IC landscape and highlights key trends related to product segmentation, company formation, revenue, and market share, latest development, and M&A activity. This report also analyzes the strategies of leading global companies with a focus on Gearbox IC portfolios and capabilities, market entry strategies, market positions, and geographic footprints, to better understand these firms' unique position in an accelerating global Gearbox IC market.

This Insight Report evaluates the key market trends, drivers, and affecting factors shaping the global outlook for Gearbox IC and breaks down the forecast by Protocol Interface, by Application, geography, and market size to highlight emerging pockets of opportunity. With a transparent methodology based on hundreds of bottom-up qualitative and quantitative market inputs, this study forecast offers a highly nuanced view of the current state and future trajectory in the global Gearbox IC.

This report presents a comprehensive overview, market shares, and growth opportunities of Gearbox IC market by product type, application, key manufacturers and key regions and countries.

Segmentation by Protocol Interface:

Ethernet Gearbox IC

PCIe Gearbox IC

CXL-Compatible Gearbox IC

Optical Module Interface Gearbox IC

Other

Segmentation by Signal Conversion Direction:

PAM4-to-NRZ Gearbox IC

NRZ-to-PAM4 Reverse Gearbox IC

Same-Rate Retiming Gearbox IC

Cross-Generation Protocol Gearbox IC

Other

Segmentation by Functional Integration:

Basic Gearbox IC

Retimer-Integrated Gearbox IC

MACsec-Integrated Gearbox IC

Crosspoint-Integrated Gearbox IC

Segmentation by Application:

Data Center Optical Module Interconnection

AI Cluster High-Speed Interconnection

Switch Line Card Port Aggregation

Active Electrical Cable Signal Conditioning

PCIe Cross-Generation Device Connection

Carrier Transport Equipment Access

Other

This report also splits the market by region:

Americas

United States

Canada

Mexico

Brazil

APAC

China

Japan

Korea

Southeast Asia

India

Australia

Europe

Germany

France

UK

Italy

Russia

Middle East & Africa

Egypt

South Africa

Israel

Turkey

GCC Countries

The below companies that are profiled have been selected based on inputs gathered from primary experts and analysing the company's coverage, product portfolio, its market penetration.

Broadcom Inc.

Marvell Technology, Inc.

MaxLinear, Inc.

Credo Technology Group Holding Ltd

Microchip Technology Inc.

Renesas Electronics Corporation

Astera Labs, Inc.

Key Questions Addressed in this Report

What is the 10-year outlook for the global Gearbox IC market?

What factors are driving Gearbox IC market growth, globally and by region?

Which technologies are poised for the fastest growth by market and region?

How do Gearbox IC market opportunities vary by end market size?

How does Gearbox IC break out by Protocol Interface, by Application?

Contents

1 SCOPE OF THE REPORT

- 1.1 Market Introduction
- 1.2 Years Considered
- 1.3 Research Objectives
- 1.4 Market Research Methodology
- 1.5 Research Process and Data Source
- 1.6 Economic Indicators
- 1.7 Currency Considered
- 1.8 Market Estimation Caveats

2 EXECUTIVE SUMMARY

- 2.1 World Market Overview
 - 2.1.1 Global Gearbox IC Annual Sales 2021-2032
 - 2.1.2 World Current & Future Analysis for Gearbox IC by Geographic Region, 2021, 2025 & 2032
 - 2.1.3 World Current & Future Analysis for Gearbox IC by Country/Region, 2021, 2025 & 2032
- 2.2 Gearbox IC Segment by Protocol Interface
 - 2.2.1 Ethernet Gearbox IC
 - 2.2.2 PCIe Gearbox IC
 - 2.2.3 CXL-Compatible Gearbox IC
 - 2.2.4 Optical Module Interface Gearbox IC
 - 2.2.5 Other
 - 2.2.6 Gearbox IC Sales by Protocol Interface
 - 2.2.6.1 Global Gearbox IC Sales Market Share by Protocol Interface (2021-2026)
 - 2.2.6.2 Global Gearbox IC Revenue and Market Share by Protocol Interface (2021-2026)
 - 2.2.6.3 Global Gearbox IC Sale Price by Protocol Interface (2021-2026)
- 2.3 Gearbox IC Segment by Signal Conversion Direction
 - 2.3.1 PAM4-to-NRZ Gearbox IC
 - 2.3.2 NRZ-to-PAM4 Reverse Gearbox IC
 - 2.3.3 Same-Rate Retiming Gearbox IC
 - 2.3.4 Cross-Generation Protocol Gearbox IC
 - 2.3.5 Other
 - 2.3.6 Gearbox IC Sales by Signal Conversion Direction

2.3.6.1 Global Gearbox IC Sales Market Share by Signal Conversion Direction (2021-2026)

2.3.6.2 Global Gearbox IC Revenue and Market Share by Signal Conversion Direction (2021-2026)

2.3.6.3 Global Gearbox IC Sale Price by Signal Conversion Direction (2021-2026)

2.4 Gearbox IC Segment by Functional Integration

2.4.1 Basic Gearbox IC

2.4.2 Retimer-Integrated Gearbox IC

2.4.3 MACsec-Integrated Gearbox IC

2.4.4 Crosspoint-Integrated Gearbox IC

2.4.5 Gearbox IC Sales by Functional Integration

2.4.5.1 Global Gearbox IC Sales Market Share by Functional Integration (2021-2026)

2.4.5.2 Global Gearbox IC Revenue and Market Share by Functional Integration (2021-2026)

2.4.5.3 Global Gearbox IC Sale Price by Functional Integration (2021-2026)

2.5 Gearbox IC Segment by Application

2.5.1 Data Center Optical Module Interconnection

2.5.2 AI Cluster High-Speed Interconnection

2.5.3 Switch Line Card Port Aggregation

2.5.4 Active Electrical Cable Signal Conditioning

2.5.5 PCIe Cross-Generation Device Connection

2.5.6 Carrier Transport Equipment Access

2.5.7 Other

2.5.8 Gearbox IC Sales by Application

2.5.8.1 Global Gearbox IC Sale Market Share by Application (2021-2026)

2.5.8.2 Global Gearbox IC Revenue and Market Share by Application (2021-2026)

2.5.8.3 Global Gearbox IC Sale Price by Application (2021-2026)

3 GLOBAL BY COMPANY

3.1 Global Gearbox IC Breakdown Data by Company

3.1.1 Global Gearbox IC Annual Sales by Company (2021-2026)

3.1.2 Global Gearbox IC Sales Market Share by Company (2021-2026)

3.2 Global Gearbox IC Annual Revenue by Company (2021-2026)

3.2.1 Global Gearbox IC Revenue by Company (2021-2026)

3.2.2 Global Gearbox IC Revenue Market Share by Company (2021-2026)

3.3 Global Gearbox IC Sale Price by Company

3.4 Key Manufacturers Gearbox IC Producing Area Distribution, Sales Area, Product Type

- 3.4.1 Key Manufacturers Gearbox IC Product Location Distribution
- 3.4.2 Players Gearbox IC Products Offered
- 3.5 Market Concentration Rate Analysis
 - 3.5.1 Competition Landscape Analysis
 - 3.5.2 Concentration Ratio (CR3, CR5 and CR10) & (2024-2026)
- 3.6 New Products and Potential Entrants
- 3.7 Market M&A Activity & Strategy

4 WORLD HISTORIC REVIEW FOR GEARBOX IC BY GEOGRAPHIC REGION

- 4.1 World Historic Gearbox IC Market Size by Geographic Region (2021-2026)
 - 4.1.1 Global Gearbox IC Annual Sales by Geographic Region (2021-2026)
 - 4.1.2 Global Gearbox IC Annual Revenue by Geographic Region (2021-2026)
- 4.2 World Historic Gearbox IC Market Size by Country/Region (2021-2026)
 - 4.2.1 Global Gearbox IC Annual Sales by Country/Region (2021-2026)
 - 4.2.2 Global Gearbox IC Annual Revenue by Country/Region (2021-2026)
- 4.3 Americas Gearbox IC Sales Growth
- 4.4 APAC Gearbox IC Sales Growth
- 4.5 Europe Gearbox IC Sales Growth
- 4.6 Middle East & Africa Gearbox IC Sales Growth

5 AMERICAS

- 5.1 Americas Gearbox IC Sales by Country
 - 5.1.1 Americas Gearbox IC Sales by Country (2021-2026)
 - 5.1.2 Americas Gearbox IC Revenue by Country (2021-2026)
- 5.2 Americas Gearbox IC Sales by Protocol Interface (2021-2026)
- 5.3 Americas Gearbox IC Sales by Application (2021-2026)
- 5.4 United States
- 5.5 Canada
- 5.6 Mexico
- 5.7 Brazil

6 APAC

- 6.1 APAC Gearbox IC Sales by Region
 - 6.1.1 APAC Gearbox IC Sales by Region (2021-2026)
 - 6.1.2 APAC Gearbox IC Revenue by Region (2021-2026)
- 6.2 APAC Gearbox IC Sales by Protocol Interface (2021-2026)

6.3 APAC Gearbox IC Sales by Application (2021-2026)

6.4 China

6.5 Japan

6.6 South Korea

6.7 Southeast Asia

6.8 India

6.9 Australia

6.10 China Taiwan

7 EUROPE

7.1 Europe Gearbox IC by Country

7.1.1 Europe Gearbox IC Sales by Country (2021-2026)

7.1.2 Europe Gearbox IC Revenue by Country (2021-2026)

7.2 Europe Gearbox IC Sales by Protocol Interface (2021-2026)

7.3 Europe Gearbox IC Sales by Application (2021-2026)

7.4 Germany

7.5 France

7.6 UK

7.7 Italy

7.8 Russia

8 MIDDLE EAST & AFRICA

8.1 Middle East & Africa Gearbox IC by Country

8.1.1 Middle East & Africa Gearbox IC Sales by Country (2021-2026)

8.1.2 Middle East & Africa Gearbox IC Revenue by Country (2021-2026)

8.2 Middle East & Africa Gearbox IC Sales by Protocol Interface (2021-2026)

8.3 Middle East & Africa Gearbox IC Sales by Application (2021-2026)

8.4 Egypt

8.5 South Africa

8.6 Israel

8.7 Turkey

8.8 GCC Countries

9 MARKET DRIVERS, CHALLENGES AND TRENDS

9.1 Market Drivers & Growth Opportunities

9.2 Market Challenges & Risks

9.3 Industry Trends

10 MANUFACTURING COST STRUCTURE ANALYSIS

10.1 Raw Material and Suppliers

10.2 Manufacturing Cost Structure Analysis of Gearbox IC

10.3 Manufacturing Process Analysis of Gearbox IC

10.4 Industry Chain Structure of Gearbox IC

11 MARKETING, DISTRIBUTORS AND CUSTOMER

11.1 Sales Channel

11.1.1 Direct Channels

11.1.2 Indirect Channels

11.2 Gearbox IC Distributors

11.3 Gearbox IC Customer

12 WORLD FORECAST REVIEW FOR GEARBOX IC BY GEOGRAPHIC REGION

12.1 Global Gearbox IC Market Size Forecast by Region

12.1.1 Global Gearbox IC Forecast by Region (2027-2032)

12.1.2 Global Gearbox IC Annual Revenue Forecast by Region (2027-2032)

12.2 Americas Forecast by Country (2027-2032)

12.3 APAC Forecast by Region (2027-2032)

12.4 Europe Forecast by Country (2027-2032)

12.5 Middle East & Africa Forecast by Country (2027-2032)

12.6 Global Gearbox IC Forecast by Protocol Interface (2027-2032)

12.7 Global Gearbox IC Forecast by Application (2027-2032)

13 KEY PLAYERS ANALYSIS

13.1 Broadcom Inc.

13.1.1 Broadcom Inc. Company Information

13.1.2 Broadcom Inc. Gearbox IC Product Portfolios and Specifications

13.1.3 Broadcom Inc. Gearbox IC Sales, Revenue, Price and Gross Margin (2021-2026)

13.1.4 Broadcom Inc. Main Business Overview

13.1.5 Broadcom Inc. Latest Developments

13.2 Marvell Technology, Inc.

- 13.2.1 Marvell Technology, Inc. Company Information
- 13.2.2 Marvell Technology, Inc. Gearbox IC Product Portfolios and Specifications
- 13.2.3 Marvell Technology, Inc. Gearbox IC Sales, Revenue, Price and Gross Margin (2021-2026)
- 13.2.4 Marvell Technology, Inc. Main Business Overview
- 13.2.5 Marvell Technology, Inc. Latest Developments
- 13.3 MaxLinear, Inc.
 - 13.3.1 MaxLinear, Inc. Company Information
 - 13.3.2 MaxLinear, Inc. Gearbox IC Product Portfolios and Specifications
 - 13.3.3 MaxLinear, Inc. Gearbox IC Sales, Revenue, Price and Gross Margin (2021-2026)
 - 13.3.4 MaxLinear, Inc. Main Business Overview
 - 13.3.5 MaxLinear, Inc. Latest Developments
- 13.4 Credo Technology Group Holding Ltd
 - 13.4.1 Credo Technology Group Holding Ltd Company Information
 - 13.4.2 Credo Technology Group Holding Ltd Gearbox IC Product Portfolios and Specifications
 - 13.4.3 Credo Technology Group Holding Ltd Gearbox IC Sales, Revenue, Price and Gross Margin (2021-2026)
 - 13.4.4 Credo Technology Group Holding Ltd Main Business Overview
 - 13.4.5 Credo Technology Group Holding Ltd Latest Developments
- 13.5 Microchip Technology Inc.
 - 13.5.1 Microchip Technology Inc. Company Information
 - 13.5.2 Microchip Technology Inc. Gearbox IC Product Portfolios and Specifications
 - 13.5.3 Microchip Technology Inc. Gearbox IC Sales, Revenue, Price and Gross Margin (2021-2026)
 - 13.5.4 Microchip Technology Inc. Main Business Overview
 - 13.5.5 Microchip Technology Inc. Latest Developments
- 13.6 Renesas Electronics Corporation
 - 13.6.1 Renesas Electronics Corporation Company Information
 - 13.6.2 Renesas Electronics Corporation Gearbox IC Product Portfolios and Specifications
 - 13.6.3 Renesas Electronics Corporation Gearbox IC Sales, Revenue, Price and Gross Margin (2021-2026)
 - 13.6.4 Renesas Electronics Corporation Main Business Overview
 - 13.6.5 Renesas Electronics Corporation Latest Developments
- 13.7 Astera Labs, Inc.
 - 13.7.1 Astera Labs, Inc. Company Information
 - 13.7.2 Astera Labs, Inc. Gearbox IC Product Portfolios and Specifications

13.7.3 Astera Labs, Inc. Gearbox IC Sales, Revenue, Price and Gross Margin
(2021-2026)

13.7.4 Astera Labs, Inc. Main Business Overview

13.7.5 Astera Labs, Inc. Latest Developments

14 RESEARCH FINDINGS AND CONCLUSION

List Of Tables

LIST OF TABLES

Table 1. Gearbox IC Annual Sales CAGR by Geographic Region (2021, 2025 & 2032) & (\$ millions)

Table 2. Gearbox IC Annual Sales CAGR by Country/Region (2021, 2025 & 2032) & (\$ millions)

Table 3. Major Players of Ethernet Gearbox IC

Table 4. Major Players of PCIe Gearbox IC

Table 5. Major Players of CXL-Compatible Gearbox IC

Table 6. Major Players of Optical Module Interface Gearbox IC

Table 7. Major Players of Other

Table 8. Global Gearbox IC Sales by Protocol Interface (2021-2026) & (Million Units)

Table 9. Global Gearbox IC Sales Market Share by Protocol Interface (2021-2026)

Table 10. Global Gearbox IC Revenue by Protocol Interface (2021-2026) & (\$ million)

Table 11. Global Gearbox IC Revenue Market Share by Protocol Interface (2021-2026)

Table 12. Global Gearbox IC Sale Price by Protocol Interface (2021-2026) & (US\$/Unit)

Table 13. Major Players of PAM4-to-NRZ Gearbox IC

Table 14. Major Players of NRZ-to-PAM4 Reverse Gearbox IC

Table 15. Major Players of Same-Rate Retiming Gearbox IC

Table 16. Major Players of Cross-Generation Protocol Gearbox IC

Table 17. Major Players of Other

Table 18. Global Gearbox IC Sales by Signal Conversion Direction (2021-2026) & (Million Units)

Table 19. Global Gearbox IC Sales Market Share by Signal Conversion Direction (2021-2026)

Table 20. Global Gearbox IC Revenue by Signal Conversion Direction (2021-2026) & (\$ million)

Table 21. Global Gearbox IC Revenue Market Share by Signal Conversion Direction (2021-2026)

Table 22. Global Gearbox IC Sale Price by Signal Conversion Direction (2021-2026) & (US\$/Unit)

Table 23. Major Players of Basic Gearbox IC

Table 24. Major Players of Retimer-Integrated Gearbox IC

Table 25. Major Players of MACsec-Integrated Gearbox IC

Table 26. Major Players of Crosspoint-Integrated Gearbox IC

Table 27. Global Gearbox IC Sales by Functional Integration (2021-2026) & (Million Units)

Table 28. Global Gearbox IC Sales Market Share by Functional Integration (2021-2026)

Table 29. Global Gearbox IC Revenue by Functional Integration (2021-2026) & (\$ million)

Table 30. Global Gearbox IC Revenue Market Share by Functional Integration (2021-2026)

Table 31. Global Gearbox IC Sale Price by Functional Integration (2021-2026) & (US\$/Unit)

Table 32. Global Gearbox IC Sale by Application (2021-2026) & (Million Units)

Table 33. Global Gearbox IC Sale Market Share by Application (2021-2026)

Table 34. Global Gearbox IC Revenue by Application (2021-2026) & (\$ million)

Table 35. Global Gearbox IC Revenue Market Share by Application (2021-2026)

Table 36. Global Gearbox IC Sale Price by Application (2021-2026) & (US\$/Unit)

Table 37. Global Gearbox IC Sales by Company (2021-2026) & (Million Units)

Table 38. Global Gearbox IC Sales Market Share by Company (2021-2026)

Table 39. Global Gearbox IC Revenue by Company (2021-2026) & (\$ millions)

Table 40. Global Gearbox IC Revenue Market Share by Company (2021-2026)

Table 41. Global Gearbox IC Sale Price by Company (2021-2026) & (US\$/Unit)

Table 42. Key Manufacturers Gearbox IC Producing Area Distribution and Sales Area

Table 43. Players Gearbox IC Products Offered

Table 44. Gearbox IC Concentration Ratio (CR3, CR5 and CR10) & (2024-2026)

Table 45. New Products and Potential Entrants

Table 46. Market M&A Activity & Strategy

Table 47. Global Gearbox IC Sales by Geographic Region (2021-2026) & (Million Units)

Table 48. Global Gearbox IC Sales Market Share Geographic Region (2021-2026)

Table 49. Global Gearbox IC Revenue by Geographic Region (2021-2026) & (\$ millions)

Table 50. Global Gearbox IC Revenue Market Share by Geographic Region (2021-2026)

Table 51. Global Gearbox IC Sales by Country/Region (2021-2026) & (Million Units)

Table 52. Global Gearbox IC Sales Market Share by Country/Region (2021-2026)

Table 53. Global Gearbox IC Revenue by Country/Region (2021-2026) & (\$ millions)

Table 54. Global Gearbox IC Revenue Market Share by Country/Region (2021-2026)

Table 55. Americas Gearbox IC Sales by Country (2021-2026) & (Million Units)

Table 56. Americas Gearbox IC Sales Market Share by Country (2021-2026)

Table 57. Americas Gearbox IC Revenue by Country (2021-2026) & (\$ millions)

Table 58. Americas Gearbox IC Sales by Protocol Interface (2021-2026) & (Million Units)

Table 59. Americas Gearbox IC Sales by Application (2021-2026) & (Million Units)

Table 60. APAC Gearbox IC Sales by Region (2021-2026) & (Million Units)

Table 61. APAC Gearbox IC Sales Market Share by Region (2021-2026)
Table 62. APAC Gearbox IC Revenue by Region (2021-2026) & (\$ millions)
Table 63. APAC Gearbox IC Sales by Protocol Interface (2021-2026) & (Million Units)
Table 64. APAC Gearbox IC Sales by Application (2021-2026) & (Million Units)
Table 65. Europe Gearbox IC Sales by Country (2021-2026) & (Million Units)
Table 66. Europe Gearbox IC Revenue by Country (2021-2026) & (\$ millions)
Table 67. Europe Gearbox IC Sales by Protocol Interface (2021-2026) & (Million Units)
Table 68. Europe Gearbox IC Sales by Application (2021-2026) & (Million Units)
Table 69. Middle East & Africa Gearbox IC Sales by Country (2021-2026) & (Million Units)
Table 70. Middle East & Africa Gearbox IC Revenue Market Share by Country (2021-2026)
Table 71. Middle East & Africa Gearbox IC Sales by Protocol Interface (2021-2026) & (Million Units)
Table 72. Middle East & Africa Gearbox IC Sales by Application (2021-2026) & (Million Units)
Table 73. Key Market Drivers & Growth Opportunities of Gearbox IC
Table 74. Key Market Challenges & Risks of Gearbox IC
Table 75. Key Industry Trends of Gearbox IC
Table 76. Gearbox IC Raw Material
Table 77. Key Suppliers of Raw Materials
Table 78. Gearbox IC Distributors List
Table 79. Gearbox IC Customer List
Table 80. Global Gearbox IC Sales Forecast by Region (2027-2032) & (Million Units)
Table 81. Global Gearbox IC Revenue Forecast by Region (2027-2032) & (\$ millions)
Table 82. Americas Gearbox IC Sales Forecast by Country (2027-2032) & (Million Units)
Table 83. Americas Gearbox IC Annual Revenue Forecast by Country (2027-2032) & (\$ millions)
Table 84. APAC Gearbox IC Sales Forecast by Region (2027-2032) & (Million Units)
Table 85. APAC Gearbox IC Annual Revenue Forecast by Region (2027-2032) & (\$ millions)
Table 86. Europe Gearbox IC Sales Forecast by Country (2027-2032) & (Million Units)
Table 87. Europe Gearbox IC Revenue Forecast by Country (2027-2032) & (\$ millions)
Table 88. Middle East & Africa Gearbox IC Sales Forecast by Country (2027-2032) & (Million Units)
Table 89. Middle East & Africa Gearbox IC Revenue Forecast by Country (2027-2032) & (\$ millions)
Table 90. Global Gearbox IC Sales Forecast by Protocol Interface (2027-2032) &

(Million Units)

Table 91. Global Gearbox IC Revenue Forecast by Protocol Interface (2027-2032) & (\$ millions)

Table 92. Global Gearbox IC Sales Forecast by Application (2027-2032) & (Million Units)

Table 93. Global Gearbox IC Revenue Forecast by Application (2027-2032) & (\$ millions)

Table 94. Broadcom Inc. Basic Information, Gearbox IC Manufacturing Base, Sales Area and Its Competitors

Table 95. Broadcom Inc. Gearbox IC Product Portfolios and Specifications

Table 96. Broadcom Inc. Gearbox IC Sales (Million Units), Revenue (\$ Million), Price (US\$/Unit) and Gross Margin (2021-2026)

Table 97. Broadcom Inc. Main Business

Table 98. Broadcom Inc. Latest Developments

Table 99. Marvell Technology, Inc. Basic Information, Gearbox IC Manufacturing Base, Sales Area and Its Competitors

Table 100. Marvell Technology, Inc. Gearbox IC Product Portfolios and Specifications

Table 101. Marvell Technology, Inc. Gearbox IC Sales (Million Units), Revenue (\$ Million), Price (US\$/Unit) and Gross Margin (2021-2026)

Table 102. Marvell Technology, Inc. Main Business

Table 103. Marvell Technology, Inc. Latest Developments

Table 104. MaxLinear, Inc. Basic Information, Gearbox IC Manufacturing Base, Sales Area and Its Competitors

Table 105. MaxLinear, Inc. Gearbox IC Product Portfolios and Specifications

Table 106. MaxLinear, Inc. Gearbox IC Sales (Million Units), Revenue (\$ Million), Price (US\$/Unit) and Gross Margin (2021-2026)

Table 107. MaxLinear, Inc. Main Business

Table 108. MaxLinear, Inc. Latest Developments

Table 109. Credo Technology Group Holding Ltd Basic Information, Gearbox IC Manufacturing Base, Sales Area and Its Competitors

Table 110. Credo Technology Group Holding Ltd Gearbox IC Product Portfolios and Specifications

Table 111. Credo Technology Group Holding Ltd Gearbox IC Sales (Million Units), Revenue (\$ Million), Price (US\$/Unit) and Gross Margin (2021-2026)

Table 112. Credo Technology Group Holding Ltd Main Business

Table 113. Credo Technology Group Holding Ltd Latest Developments

Table 114. Microchip Technology Inc. Basic Information, Gearbox IC Manufacturing Base, Sales Area and Its Competitors

Table 115. Microchip Technology Inc. Gearbox IC Product Portfolios and Specifications

Table 116. Microchip Technology Inc. Gearbox IC Sales (Million Units), Revenue (\$ Million), Price (US\$/Unit) and Gross Margin (2021-2026)

Table 117. Microchip Technology Inc. Main Business

Table 118. Microchip Technology Inc. Latest Developments

Table 119. Renesas Electronics Corporation Basic Information, Gearbox IC Manufacturing Base, Sales Area and Its Competitors

Table 120. Renesas Electronics Corporation Gearbox IC Product Portfolios and Specifications

Table 121. Renesas Electronics Corporation Gearbox IC Sales (Million Units), Revenue (\$ Million), Price (US\$/Unit) and Gross Margin (2021-2026)

Table 122. Renesas Electronics Corporation Main Business

Table 123. Renesas Electronics Corporation Latest Developments

Table 124. Astera Labs, Inc. Basic Information, Gearbox IC Manufacturing Base, Sales Area and Its Competitors

Table 125. Astera Labs, Inc. Gearbox IC Product Portfolios and Specifications

Table 126. Astera Labs, Inc. Gearbox IC Sales (Million Units), Revenue (\$ Million), Price (US\$/Unit) and Gross Margin (2021-2026)

Table 127. Astera Labs, Inc. Main Business

Table 128. Astera Labs, Inc. Latest Developments

List Of Figures

LIST OF FIGURES

- Figure 1. Picture of Gearbox IC
- Figure 2. Gearbox IC Report Years Considered
- Figure 3. Research Objectives
- Figure 4. Research Methodology
- Figure 5. Research Process and Data Source
- Figure 6. Global Gearbox IC Sales Growth Rate 2021-2032 (Million Units)
- Figure 7. Global Gearbox IC Revenue Growth Rate 2021-2032 (\$ millions)
- Figure 8. Gearbox IC Sales by Geographic Region (2021, 2025 & 2032) & (\$ millions)
- Figure 9. Gearbox IC Sales Market Share by Country/Region (2025)
- Figure 10. Gearbox IC Sales Market Share by Country/Region (2021, 2025 & 2032)
- Figure 11. Product Picture of Ethernet Gearbox IC
- Figure 12. Product Picture of PCIe Gearbox IC
- Figure 13. Product Picture of CXL-Compatible Gearbox IC
- Figure 14. Product Picture of Optical Module Interface Gearbox IC
- Figure 15. Product Picture of Other
- Figure 16. Global Gearbox IC Sales Market Share by Protocol Interface in 2026
- Figure 17. Global Gearbox IC Revenue Market Share by Protocol Interface (2021-2026)
- Figure 18. Product Picture of PAM4-to-NRZ Gearbox IC
- Figure 19. Product Picture of NRZ-to-PAM4 Reverse Gearbox IC
- Figure 20. Product Picture of Same-Rate Retiming Gearbox IC
- Figure 21. Product Picture of Cross-Generation Protocol Gearbox IC
- Figure 22. Product Picture of Other
- Figure 23. Global Gearbox IC Sales Market Share by Signal Conversion Direction in 2026
- Figure 24. Global Gearbox IC Revenue Market Share by Signal Conversion Direction (2021-2026)
- Figure 25. Product Picture of Basic Gearbox IC
- Figure 26. Product Picture of Retimer-Integrated Gearbox IC
- Figure 27. Product Picture of MACsec-Integrated Gearbox IC
- Figure 28. Product Picture of Crosspoint-Integrated Gearbox IC
- Figure 29. Global Gearbox IC Sales Market Share by Functional Integration in 2026
- Figure 30. Global Gearbox IC Revenue Market Share by Functional Integration (2021-2026)
- Figure 31. Gearbox IC Consumed in Data Center Optical Module Interconnection
- Figure 32. Global Gearbox IC Market: Data Center Optical Module Interconnection

(2021-2026) & (Million Units)

Figure 33. Gearbox IC Consumed in AI Cluster High-Speed Interconnection

Figure 34. Global Gearbox IC Market: AI Cluster High-Speed Interconnection

(2021-2026) & (Million Units)

Figure 35. Gearbox IC Consumed in Switch Line Card Port Aggregation

Figure 36. Global Gearbox IC Market: Switch Line Card Port Aggregation (2021-2026) & (Million Units)

Figure 37. Gearbox IC Consumed in Active Electrical Cable Signal Conditioning

Figure 38. Global Gearbox IC Market: Active Electrical Cable Signal Conditioning (2021-2026) & (Million Units)

Figure 39. Gearbox IC Consumed in PCIe Cross-Generation Device Connection

Figure 40. Global Gearbox IC Market: PCIe Cross-Generation Device Connection (2021-2026) & (Million Units)

Figure 41. Gearbox IC Consumed in Carrier Transport Equipment Access

Figure 42. Global Gearbox IC Market: Carrier Transport Equipment Access (2021-2026) & (Million Units)

Figure 43. Gearbox IC Consumed in Other

Figure 44. Global Gearbox IC Market: Other (2021-2026) & (Million Units)

Figure 45. Global Gearbox IC Sale Market Share by Application (2025)

Figure 46. Global Gearbox IC Revenue Market Share by Application in 2025

Figure 47. Gearbox IC Sales by Company in 2025 (Million Units)

Figure 48. Global Gearbox IC Sales Market Share by Company in 2025

Figure 49. Gearbox IC Revenue by Company in 2025 (\$ millions)

Figure 50. Global Gearbox IC Revenue Market Share by Company in 2025

Figure 51. Global Gearbox IC Sales Market Share by Geographic Region (2021-2026)

Figure 52. Global Gearbox IC Revenue Market Share by Geographic Region in 2025

Figure 53. Americas Gearbox IC Sales 2021-2026 (Million Units)

Figure 54. Americas Gearbox IC Revenue 2021-2026 (\$ millions)

Figure 55. APAC Gearbox IC Sales 2021-2026 (Million Units)

Figure 56. APAC Gearbox IC Revenue 2021-2026 (\$ millions)

Figure 57. Europe Gearbox IC Sales 2021-2026 (Million Units)

Figure 58. Europe Gearbox IC Revenue 2021-2026 (\$ millions)

Figure 59. Middle East & Africa Gearbox IC Sales 2021-2026 (Million Units)

Figure 60. Middle East & Africa Gearbox IC Revenue 2021-2026 (\$ millions)

Figure 61. Americas Gearbox IC Sales Market Share by Country in 2025

Figure 62. Americas Gearbox IC Revenue Market Share by Country (2021-2026)

Figure 63. Americas Gearbox IC Sales Market Share by Protocol Interface (2021-2026)

Figure 64. Americas Gearbox IC Sales Market Share by Application (2021-2026)

Figure 65. United States Gearbox IC Revenue Growth 2021-2026 (\$ millions)

- Figure 66. Canada Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 67. Mexico Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 68. Brazil Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 69. APAC Gearbox IC Sales Market Share by Region in 2025
- Figure 70. APAC Gearbox IC Revenue Market Share by Region (2021-2026)
- Figure 71. APAC Gearbox IC Sales Market Share by Protocol Interface (2021-2026)
- Figure 72. APAC Gearbox IC Sales Market Share by Application (2021-2026)
- Figure 73. China Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 74. Japan Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 75. South Korea Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 76. Southeast Asia Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 77. India Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 78. Australia Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 79. China Taiwan Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 80. Europe Gearbox IC Sales Market Share by Country in 2025
- Figure 81. Europe Gearbox IC Revenue Market Share by Country (2021-2026)
- Figure 82. Europe Gearbox IC Sales Market Share by Protocol Interface (2021-2026)
- Figure 83. Europe Gearbox IC Sales Market Share by Application (2021-2026)
- Figure 84. Germany Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 85. France Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 86. UK Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 87. Italy Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 88. Russia Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 89. Middle East & Africa Gearbox IC Sales Market Share by Country (2021-2026)
- Figure 90. Middle East & Africa Gearbox IC Sales Market Share by Protocol Interface (2021-2026)
- Figure 91. Middle East & Africa Gearbox IC Sales Market Share by Application (2021-2026)
- Figure 92. Egypt Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 93. South Africa Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 94. Israel Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 95. Turkey Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 96. GCC Countries Gearbox IC Revenue Growth 2021-2026 (\$ millions)
- Figure 97. Manufacturing Cost Structure Analysis of Gearbox IC in 2026
- Figure 98. Manufacturing Process Analysis of Gearbox IC
- Figure 99. Industry Chain Structure of Gearbox IC
- Figure 100. Channels of Distribution
- Figure 101. Global Gearbox IC Sales Market Forecast by Region (2027-2032)

Figure 102. Global Gearbox IC Revenue Market Share Forecast by Region (2027-2032)

Figure 103. Global Gearbox IC Sales Market Share Forecast by Protocol Interface
(2027-2032)

Figure 104. Global Gearbox IC Revenue Market Share Forecast by Protocol Interface
(2027-2032)

Figure 105. Global Gearbox IC Sales Market Share Forecast by Application
(2027-2032)

Figure 106. Global Gearbox IC Revenue Market Share Forecast by Application
(2027-2032)

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