

Global Fan-Out Wafer Level Packaging Market Growth (Status and Outlook) 2025-2031

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Abstracts

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The global Fan-Out Wafer Level Packaging market size is predicted to grow from US\$ 1928 million in 2025 to US\$ 6005 million in 2031; it is expected to grow at a CAGR of 20.9% from 2025 to 2031.

The Fan-Out WLP technique involves cutting and separating the chip and then embedding the chip inside the panel. The procedure is to attach the chip face down to the Carrier, and the chip spacing should conform to the Pitch specification of the circuit design, while the receiver performs Molding to form a Panel. Follow-up will be separation, sealant panel and a vehicle for sealant panel Wafer shape, also called reconstruct Wafer (Reconstituted Wafer), can be widely used standard Wafer process, need is formed on the sealant panel circuit design. Since the area of the sealing panel is larger than that of the chip, not only can I/O contacts be made into the wafer area by Fan-In method; It can also be Fanned Out on a plastic mold to accommodate more I/O contacts.

The industry's leading producers are TSMC, ASE Technology Holding Co., and JCET Group, which accounted for 44.97%, 16.03% and 11.81% of revenue in 2019, respectively.

LPI (LP Information)' newest research report, the "Fan-Out Wafer Level Packaging Industry Forecast" looks at past sales and reviews total world Fan-Out Wafer Level Packaging sales in 2024, providing a comprehensive analysis by region and market sector of projected Fan-Out Wafer Level Packaging sales for 2025 through 2031. With Fan-Out Wafer Level Packaging sales broken down by region, market sector and sub-

sector, this report provides a detailed analysis in US\$ millions of the world Fan-Out Wafer Level Packaging industry.

This Insight Report provides a comprehensive analysis of the global Fan-Out Wafer Level Packaging landscape and highlights key trends related to product segmentation, company formation, revenue, and market share, latest development, and M&A activity. This report also analyses the strategies of leading global companies with a focus on Fan-Out Wafer Level Packaging portfolios and capabilities, market entry strategies, market positions, and geographic footprints, to better understand these firms' unique position in an accelerating global Fan-Out Wafer Level Packaging market.

This Insight Report evaluates the key market trends, drivers, and affecting factors shaping the global outlook for Fan-Out Wafer Level Packaging and breaks down the forecast by Type, by Application, geography, and market size to highlight emerging pockets of opportunity. With a transparent methodology based on hundreds of bottom-up qualitative and quantitative market inputs, this study forecast offers a highly nuanced view of the current state and future trajectory in the global Fan-Out Wafer Level Packaging.

This report presents a comprehensive overview, market shares, and growth opportunities of Fan-Out Wafer Level Packaging market by product type, application, key players and key regions and countries.

Segmentation by Type:

High Density Fan-Out Package

Core Fan-Out Package

Segmentation by Application:

CMOS Image Sensor

A Wireless Connection

Logic and Memory Integrated Circuits

Mems and Sensors

Analog and Hybrid Integrated Circuits

Others

This report also splits the market by region:

Americas

United States

Canada

Mexico

Brazil

APAC

China

Japan

Korea

Southeast Asia

India

Australia

Europe

Germany

France

UK

Italy

Russia

Middle East & Africa

Egypt

South Africa

Israel

Turkey

GCC Countries

The below companies that are profiled have been selected based on inputs gathered from primary experts and analyzing the company's coverage, product portfolio, its market penetration.

TSMC

ASE Technology Holding Co.

JCET Group

Amkor Technology

Siliconware Technology (SuZhou) Co.

Nepes

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