

# Electronic Design Automation (EDA) Tools Market - Forecast from 2026 to 2031

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## Abstracts

Electronic Design Automation Tools (EDA) Market is forecasted to rise at a 9.72% CAGR, reaching USD 25.709 billion in 2031 from USD 14.736 billion in 2025.

Electronic Design Automation (EDA) tools encompass software suites for the conceptualization, synthesis, simulation, verification, and optimization of integrated circuits (ICs), system-on-chips (SoCs), and printed circuit boards (PCBs). These platforms leverage algorithms for logic synthesis, place-and-route, timing analysis, power integrity, and thermal modeling to address the escalating complexity of sub-3 nm nodes, heterogeneous integration, and multi-die packages. The market, valued at USD 16.78 billion in 2025 (Straits Research, 2025), is projected to reach USD 34.58 billion by 2033 at a CAGR of 9.46%, driven by AI/ML-infused workflows and the proliferation of edge-AI, 5G, and automotive SoCs.

### Segmentation Insights

**By Type:** Semiconductor Intellectual Property (SIP) cores—pre-verified, reusable blocks for processors, interfaces, and accelerators—command the largest share, enabling 30–50% reductions in design cycles for complex ASICs. Demand surges for ARM-based IP in mobile and automotive applications, alongside RISC-V open-source variants for cost-sensitive IoT.

**By Deployment:** On-premises solutions retain dominance (65% share), favored for IP security in defense and high-volume fabs where network latency could compromise simulation fidelity. However, cloud-based platforms are gaining at 9.72% CAGR through 2032 (Data Bridge Market Research, 2025), offering elastic compute for exploratory design and collaborative verification.

**By Application:** Consumer electronics leads, propelled by miniaturization in smartphones, wearables, and smart appliances requiring compact, low-power ICs. The automotive segment exhibits the fastest growth (9.72% CAGR to 2032), as ADAS, infotainment, and EV powertrains demand ISO 26262-compliant tools for functional safety and mixed-signal verification.

**By Region:** Asia-Pacific accelerates at 9.72% CAGR to 2032 (Persistence Market Research, 2025), holding 32% share in 2025, anchored by TSMC, Samsung, and SMIC's advanced-node ramps (A16, N2P). North America follows with 25–30% share, bolstered by Intel/AMD R&D and U.S. CHIPS Act subsidies exceeding USD 52 billion for domestic fabs.

## Top Trends

1. **Cloud-Based EDA Adoption:** Scalable, pay-per-use models reduce capex by 40–60% for SMEs, enabling remote collaboration and burst compute for large-scale simulations. Integration with hyperscalers (AWS, Azure) supports AI-accelerated flows, with 38% market penetration projected by 2025 (Persistence Market Research, 2025).

2. **5G and Edge Computing Proliferation:** Deployment of 1.8 billion 5G connections by mid-2025 (Global Market Insights, 2025) demands EDA for low-latency RF/mmWave ICs and heterogeneous SoCs with advanced packaging (2.5D/3D). Tools for thermal-aware interconnects and backside power delivery are critical for edge-AI accelerators.

## Growth Drivers vs. Challenges

### Drivers:

**IC and Chip Design Complexity:** Transition to 2 nm/1.6 nm nodes (TSMC N2P/A16) requires EDA for transistor-level optimization, with Synopsys/Cadence flows certified for photonic integration and angstrom-scale processes (April 2025). AI/ML-embedded tools automate PPA (power, performance, area) trade-offs, cutting turnaround by 50% and re-spin costs exceeding USD 50 million per tape-out.

**Consumer Electronics and Miniaturization:** Global disposable income per capita rises to USD 10,677 in 2025 (EIA/IEO, 2023 projection), fueling demand for compact PCBs in wearables and smart homes. EDA streamlines high-density

interconnects, error detection, and productivity gains, accelerating time-to-market for 5G-enabled devices.

### Challenges:

**High Initial Investment and Licensing:** Advanced suites demand USD 1–5 million annual licenses plus training, deterring SMEs and startups. Total ownership costs, including maintenance and compute infrastructure, limit adoption in cost-sensitive regions, capping market penetration below 70% for premium tools.

### Regional Analysis

**North America:** Holds 25–30% share through innovation hubs (Qualcomm, Intel, AMD) and CHIPS Act incentives. Automotive electrification and defense ICs drive verification demand, with cloud-hybrid models emerging for agile R&D.

**Asia-Pacific:** Fastest-growing at 32% share in 2025, led by China's fab expansions and Taiwan/South Korea's leadership in AI/HPC chips. Samsung/TSMC collaborations with EDA vendors ensure node-specific flows, amplified by EV and 5G hardware surges.

### Competitive Landscape

The fragmented oligopoly features Synopsys (25% share), Cadence (20%), Siemens EDA (15%), ANSYS, Keysight, Altium, Zuken, and Silvaco. Consolidation accelerates: Synopsys' USD 35 billion Ansys acquisition (2025 completion) unifies multi-physics simulation, while Siemens' October 2024 Altair buy integrates HPC and data analytics for system-level design. Focus areas include AI-driven optimization, open-source RISC-V support, and angstrom-node certification to counter export controls and parallel ecosystems.

### Key Benefits of this Report:

**Insightful Analysis:** Gain detailed market insights covering major as well as emerging geographical regions, focusing on customer segments, government policies and socio-economic factors, consumer preferences, industry verticals, and other sub-segments.

**Competitive Landscape:** Understand the strategic maneuvers employed by key players globally to understand possible market penetration with the correct strategy.

**Market Drivers & Future Trends:** Explore the dynamic factors and pivotal market trends and how they will shape future market developments.

**Actionable Recommendations:** Utilize the insights to exercise strategic decisions to uncover new business streams and revenues in a dynamic environment.

**Caters to a Wide Audience:** Beneficial and cost-effective for startups, research institutions, consultants, SMEs, and large enterprises.

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Report Coverage:

Historical data from 2021 to 2025 & forecast data from 2026 to 2031

Growth Opportunities, Challenges, Supply Chain Outlook, Regulatory Framework, and Trend Analysis

Competitive Positioning, Strategies, and Market Share Analysis

Revenue Growth and Forecast Assessment of segments and regions including countries

Company Profiling (Strategies, Products, Financial Information, and Key Developments among others.

Global Electronic Design Automation (EDA) Tool Market is analyzed into the following segments:

## By Type

Semiconductor Intellectual Property (SIP)

IC Physical Design and Verification

Computer Aided Engineering (CAE)

Printed Circuit Board & Multi-Chip Module (PCB & MCM)

Others

## By Deployment

On-Premise

Cloud

## By Application

Consumer Electronics

Automotive

Manufacturing

Telecommunication

Others

## By Geography

North America

United States

Canada

Mexico

South America

Brazil

Argentina

Others

Europe

United Kingdom

Germany

France

Italy

Spain

Others

Middle East and Africa

Saudi Arabia

UAE

Others

Asia Pacific

Japan

China

India

South Korea

Taiwan

Thailand

Indonesia

Others

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