

3D Semiconductor Packaging Market - Forecasts from 2019 to 2024

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Abstracts

The three-dimensional integrated circuits (ICs) are integrated circuits manufactured using a new packaging technology of stacking silicon wafers and interconnecting them vertically using Through Silicon Vias (TSVs) or Cu-Cu connections, so that they behave as a single device, achieving improved performance at reduced power and smaller footprint than two-dimensional processes. The 3D semiconductor packaging market is expected to grow at a significant CAGR of 14.46% to reach a market size of US\$6.044 billion in 2024 from US\$2.688 billion in 2018. As the demand for higher capacity electronic devices with more efficient power consumption increases, it drives the need to implement 3D ICs in various such devices.

DRIVERS

Increasing global demand for high-end electronic devices using miniaturized circuits with low power consumption and reduced size.

Heavy investments on the R&D by many key industry players.

RESTRAINTS

Competition from already established tech giants who are heavily investing in this area.

Lack of clarity regarding standardization and ownership concerns

RECENT DEVELOPMENTS

In 2015, Jiangsu Chanjiang Electronics Technology Co. Ltd acquired Statschippac to



augment its R&D capabilities.

ASE Group is considering a merger with SPIL. Segmentation The 3D Semiconductor packaging market has been analyzed through the following segments: By Technology Through Silicon Vias (TSV) Fan Out Wafer Level Packaging Wire Bonding Others By Industry Vertical Electronics Communication and Technology Manufacturing Automotive Defense and Aerospace Healthcare Others By Material

Bonding Wire



Lead frame	
Organic Substrate	
Encapsulation Resin	
Ceramic Package	
Die Attach Material	
Others	
By Geography	
North America	
USA	
Canada	
Others	
South America	
Brazil	
Argentina	
Others	
Europe	
United Kingdom	
Germany	
France	
Others	

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Middle East and Africa
Israel
UAE
Saudi Arabia
Others
Asia Pacific
China
Japan
South Korea
India
Others



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