

Global Wafer-Level Silicon Photonics Test System Supply, Demand and Key Producers, 2026-2032

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Abstracts

The global Wafer-Level Silicon Photonics Test System market size is expected to reach \$ 1114 million by 2032, rising at a market growth of 21.3% CAGR during the forecast period (2026-2032).

A Wafer-Level Silicon Photonics Test System is a dedicated wafer-level electro-optical test platform used to characterize, screen, and qualify silicon photonics devices, photonic integrated circuits, and related optoelectronic integrated chips before packaging. The scope of this study focuses on integrated test systems deployed at wafer, reticle, bar, or bare-die stages. A typical system combines a semi-automatic or fully automatic wafer prober, optical fiber or fiber-array coupling hardware, six-axis precision positioning and active optical alignment, electrical and RF probing, tunable lasers, optical power meters, polarization control, source-measure units, high-speed electrical instruments, temperature-controlled chucks, light-tight enclosures, machine vision, calibration algorithms, test automation software, data management, and factory automation interfaces. Its core functions include optical coupling, optical-electrical and electrical-optical measurement, passive photonic spectral characterization, active device LIV / EO / OE testing, RF and high-speed validation, process control monitoring, known-good-die identification, yield feedback, and production screening for silicon photonics foundries, IDMs, optical module makers, co-packaged optics suppliers, AI data-center optical interconnect manufacturers, and integrated photonics R&D platforms.

Based on our research, the wafer-level silicon photonics test system market should not be viewed as a simple extension of conventional electronic wafer probing. It is a cross-domain equipment segment that combines semiconductor test automation, precision optical coupling, electro-optical and RF measurement, active alignment, thermal control,

calibration algorithms, and production data infrastructure. Conventional IC wafer test mainly focuses on electrical contact, pin count, parallelism, and parametric screening, while silicon photonics wafer test must also solve fiber-to-waveguide coupling, grating or edge-coupler alignment, polarization control, optical power stability, insertion loss repeatability, reflection effects, temperature drift, and high-speed optical-electrical correlation. For this reason, this study adopts a narrow revenue scope. General-purpose optical instruments, generic probers, packaged optical module testers, and testing services are not treated as core revenue unless they are delivered as part of a wafer-level silicon photonics test system. The broader supplier pool, however, still includes critical component suppliers and system integrators because the industry remains ecosystem-driven and project-based.

Demand is shifting from research labs and MPW characterization toward pilot production and early high-volume manufacturing. Before 2025, most demand came from silicon photonics foundries, IDMs, academic platforms, optical module companies, and early CPO programs. Starting in 2025-2026, AI data centers, 800G/1.6T optical interconnects, co-packaged optics, near-package optics, optical I/O, and hybrid-bonded PIC/EIC architectures are increasing the need for wafer-level screening. The economic driver is straightforward: once a photonic die is diced, assembled, fiber-attached, or co-packaged with electronic ICs, the cost of failure rises sharply. Wafer-level electro-optical screening therefore becomes a critical enabler of known-good-die selection, yield learning, process control, and cost reduction.

From a technology-roadmap perspective, three product families are likely to coexist. The first is flexible R&D and pilot-production PIC wafer or die test stations, which emphasize multi-device compatibility, rapid configuration, and support for both surface and edge coupling. The second is 200 mm and 300 mm automated wafer-level test systems for foundries and IDMs, which emphasize throughput, repeatability, thermal stability, factory automation, and traceable data. The third is high-volume double-sided electro-optical test cells and wafer-level burn-in or reliability systems for CPO, optical engines, and optical I/O devices. Edge coupling, grating coupling, wafer-level edge coupling, double-sided probing, fiber-array parallelism, RF-optical co-test, and automated calibration will become the key differentiators. The industry will remain customized in the near term, but the direction is clearly toward modularity, software-defined workflows, and open ecosystems that reduce integration burden for production customers.

From the competitive trend perspective, the silicon photonics wafer test system market is expected to move from customized engineering setups toward more standardized,

production-ready test cells. In the early stage, many systems were assembled through a combination of a wafer prober, optical instruments, precision alignment stages, and customer-specific software. As silicon photonics, CPO, and optical I/O move closer to high-volume manufacturing, customers will increasingly require integrated platforms with higher throughput, better repeatability, automated optical alignment, double-sided probing capability, factory automation interfaces, and traceable production data. This transition favors vendors that can combine semiconductor ATE experience, photonics alignment expertise, optical-electrical measurement capability, and global service support. At the same time, regional suppliers, especially in China and Taiwan, are likely to gain share in engineering systems, pilot lines, and localized production support. Over the next few years, competition will not be determined only by instrument accuracy or prober performance, but by the ability to deliver a stable, scalable, and software-driven wafer-level test workflow. The market is therefore likely to evolve into a layered structure: a small group of global platform suppliers serving advanced HVM customers, several specialized photonics automation and probe-system vendors serving both R&D and production customers, and a broader group of regional integrators and component suppliers supporting localized applications.

This report studies the global Wafer-Level Silicon Photonics Test System demand, key companies, and key regions.

This report is a detailed and comprehensive analysis of the world market for Wafer-Level Silicon Photonics Test System, and provides market size (US\$ million) and Year-over-Year (YoY) growth, considering 2025 as the base year. This report explores demand trends and competition, as well as details the characteristics of Wafer-Level Silicon Photonics Test System that contribute to its increasing demand across many markets.

Highlights and key features of the study

Global Wafer-Level Silicon Photonics Test System total market, 2021-2032, (USD Million)

Global Wafer-Level Silicon Photonics Test System total market by region & country, CAGR, 2021-2032, (USD Million)

U.S. VS China: Wafer-Level Silicon Photonics Test System total market, key domestic companies, and share, (USD Million)

Global Wafer-Level Silicon Photonics Test System revenue by player, revenue and market share 2021-2026, (USD Million)

Global Wafer-Level Silicon Photonics Test System total market by Type, CAGR, 2021-2032, (USD Million)

Global Wafer-Level Silicon Photonics Test System total market by Application, CAGR, 2021-2032, (USD Million)

This report profiles major players in the global Wafer-Level Silicon Photonics Test System market based on the following parameters - company overview, revenue, gross margin, product portfolio, geographical presence, and key developments. Key companies covered as a part of this study include Keysight Technologies, Inc., Teradyne, Inc., FormFactor, Inc., Advantest Corporation, Tokyo Electron Limited, MPI Corporation, RoboTechnik Intelligent Technology Co., Ltd., EXFO Inc., Semight Instruments Co., Ltd., SEMISHARE CO., LTD., etc.

This report also provides key insights about market drivers, restraints, opportunities, new product launches or approvals.

Stakeholders would have ease in decision-making through various strategy matrices used in analyzing the world Wafer-Level Silicon Photonics Test System market

Detailed Segmentation:

Each section contains quantitative market data including market by value (US\$ Millions), by player, by regions, by Type, and by Application. Data is given for the years 2021-2032 by year with 2025 as the base year, 2026 as the estimate year, and 2027-2032 as the forecast year.

Global Wafer-Level Silicon Photonics Test System Market, By Region:

United States

China

Europe

Japan

South Korea

ASEAN

India

Rest of World

Global Wafer-Level Silicon Photonics Test System Market, Segmentation by Type:

Integrated Wafer Test System

Other

Global Wafer-Level Silicon Photonics Test System Market, Segmentation by Wafer / Device Format:

6-inch and Below Wafer Test

8-inch Wafer Test

12-inch Wafer Test

Other

Global Wafer-Level Silicon Photonics Test System Market, Segmentation by Automation Level:

Manual Test System

Semi-Automated Test System

Fully Automated Wafer Test System

Global Wafer-Level Silicon Photonics Test System Market, Segmentation by Measurement Configuration:

Optical-Only Configuration

Electrical-Only Configuration

Optical-to-Electrical Configuration

Electrical-to-Optical Configuration

Other

Global Wafer-Level Silicon Photonics Test System Market, Segmentation by Application:

R&D Characterization

Process Monitoring

Production Screening

Failure Analysis Support

Other

Companies Profiled:

Keysight Technologies, Inc.

Teradyne, Inc.

FormFactor, Inc.

Advantest Corporation

Tokyo Electron Limited

MPI Corporation

RoboTechnik Intelligent Technology Co., Ltd.

EXFO Inc.

Semight Instruments Co., Ltd.

SEMISHARE CO., LTD.

STAr Technologies, Inc.

FIBERPRO, Inc.

SPEA S.p.A.

Aehr Test Systems

Enlitech

Yonata Electronics Co., Ltd.

Key Questions Answered

1. How big is the global Wafer-Level Silicon Photonics Test System market?
2. What is the demand of the global Wafer-Level Silicon Photonics Test System market?
3. What is the year over year growth of the global Wafer-Level Silicon Photonics Test System market?
4. What is the total value of the global Wafer-Level Silicon Photonics Test System market?
5. Who are the Major Players in the global Wafer-Level Silicon Photonics Test System market?
6. What are the growth factors driving the market demand?

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