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Global Single Photon Avalanche Diode (SPAD) Module Supply, Demand and Key Producers, 2026-2032

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Abstracts

The global Single Photon Avalanche Diode (SPAD) Module market size is expected to reach $ 2408 million by 2032, rising at a market growth of 12.9% CAGR during the forecast period (2026-2032).

In 2025, global sales volume for Single Photon Avalanche Diode (SPAD) modules reached 383.31 million units, with an average price of $2.48 per unit.

A Single Photon Avalanche Diode (SPAD) is a highly sensitive solid-state photodetector. It operates at a reverse-bias voltage above its breakdown voltage (known as ?Geiger mode?). This allows a single incoming photon to trigger a massive, self-sustaining avalanche of electrons, acting as a highly precise, digital ?click? for ultra-low light detection.

The SPAD sensor-level market refers to the market for sensing and detection units based on Single Photon Avalanche Diode (SPAD) technology. The scope includes SPAD sensors, SPAD detector devices, SPAD arrays, SPAD-based ToF/dToF sensor modules, and single-photon counting detector modules. To avoid double counting across the value chain from bare die to packaged device and module, the market is measured at the sensor-level product that is sold externally as an independent sensing or detection unit. Internally consumed SPAD bare dies, wafers, packaged components used in downstream modules, and complete downstream systems such as cameras, LiDAR systems, TCSPC instruments, smartphones, robots, and vehicles are excluded from direct market value calculation. Wafer-level and bare-die capacity data are used only as a cross-check for shipment and revenue estimates.

The raw material ecosystem for SPADs centers on semiconductor wafer substrates,

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supplemented by materials such as epitaxial layers, specialty gases, photoresists, and metal targets. Silicon-based SPADs utilize high-resistivity silicon wafers (typically 8 or 12 inches) as substrates and are manufactured using CMOS-compatible processes; they share an upstream material supply chain with mainstream integrated circuits, a key advantage that enables lower costs and mass production. In contrast, InGaAs/InP SPADs require Indium Phosphide (InP) substrates and Indium Gallium Arsenide (InGaAs) epitaxial layers; these III-V compound semiconductor materials are difficult to grow, come in smaller wafer sizes (typically 2?4 inches), and suffer from low yields, resulting in raw material costs that are significantly higher than those of silicon-based products. Germanium-based SPADs involve growing a germanium epitaxial layer on a silicon substrate, thereby combining infrared detection capabilities with the integration advantages of the silicon platform. Specialty gases (such as silane, phosphine, and arsine) are used in epitaxial growth and doping processes, while photoresists and metal targets (aluminum, copper, tungsten, etc.) are employed for patterning and interconnection. Additionally, packaging materials (ceramic substrates, epoxy resins, gold/copper bonding wires, etc.) and testing equipment (single-photon sources, time-correlated single-photon counters, etc.) constitute significant cost components. As SPAD technology evolves toward higher integration and larger arrays, requirements for wafer quality and process control have become increasingly stringent, leading to an upward trend in the proportion of raw material costs. In terms of cost structure, wafer fabrication and raw materials constitute the primary expenses for SPADs, typically accounting for 40%?55% of the total cost. Silicon-based SPADs benefit from compatibility with CMOS processes, resulting in relatively low wafer costs (approximately $500?$1,000 per 8-inch silicon wafer). In contrast, InGaAs/InP-SPADs incur extremely high costs for InP substrates and InGaAs epitaxial layers?with 2-inch InP wafers costing thousands of dollars?making them several to dozens of times more expensive than their silicon counterparts. Manufacturing process costs account for approximately 25%?35%; SPAD production involves dozens of steps, including epitaxial growth, ion implantation, photolithography, etching, thin-film deposition, CMP, and metallization. Critical processes such as avalanche region formation, quenching circuit integration, and deep trench isolation (DTI) demand exceptionally high equipment precision and cleanroom standards, leading to significant equipment depreciation and operating expenses. Packaging and testing costs represent about 15%?25% of the total. SPADs require high standards for hermeticity, heat dissipation, and electromagnetic shielding; large-array products, in particular, necessitate wafer-level or 3D-stacked packaging, which significantly drives up costs. The testing phase requires expensive instrumentation?such as single-photon sources and picosecond-resolution equipment?and involves long testing times and rigorous yield screening. Research, development, and design costs account for 5%?10%. SPAD design is multidisciplinary,

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integrating device physics, circuit design, and optical simulation, and entails high intellectual property (IP) costs, with a cumulative total of 6,780 licensed patents directly related to SPAD technology worldwide. Yield loss represents a hidden yet significant cost factor; yields for high-end, low-noise devices (dark count rate

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