

Global Semiconductor Wafer Polishing Pad Supply, Demand and Key Producers, 2026-2032

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Abstracts

The global Semiconductor Wafer Polishing Pad market size is expected to reach \$ 1975 million by 2032, rising at a market growth of 6.5% CAGR during the forecast period (2026-2032).

A Semiconductor Wafer Polishing Pad is a key consumable material used in the Chemical Mechanical Polishing (CMP) process for semiconductor manufacturing. It is mainly used to planarize the surfaces of single-crystal silicon wafers, dielectric layers, and metal interconnect layers during integrated circuit fabrication. During CMP, the polishing pad stores and distributes slurry across the wafer surface, maintains stable contact between the wafer and the slurry, transfers the mechanical energy required for material removal, removes polishing residues, and helps maintain the mechanical and chemical environment required for stable polishing. The pad's material structure, porosity, hardness, compressibility, surface texture, and wear resistance directly affect material removal rate, wafer surface planarity, defect control, and process stability, making it an essential consumable that determines wafer polishing quality and production efficiency. In 2025, global CMP polishing pad output reached 2.70 million pieces, with an average selling price of USD 453 per piece.

The semiconductor wafer polishing pad industry is a critical part of the Chemical Mechanical Polishing (CMP) value chain. Polishing pads are used to planarize the surfaces of silicon wafers, dielectric layers, metal interconnect layers, barrier layers, and advanced compound semiconductor wafers such as silicon carbide. As advanced logic, memory, high-performance computing, power semiconductors, and compound semiconductor devices continue to develop, wafer manufacturers are placing increasingly stringent requirements on surface planarity, defect control, material removal stability, and polishing uniformity. This is driving CMP pads from standard

consumables toward high-performance, process-specific, and highly customized materials. In terms of product structure, CMP polishing pads mainly include polyurethane pads, non-woven pads, composite pads, and high-performance pads designed for specific materials and processes. Different applications, such as silicon wafer polishing, oxide CMP, copper interconnect CMP, tungsten CMP, barrier layer CMP, and SiC wafer polishing, require different pad hardness, pore structure, compressibility, surface groove design, wear resistance, and slurry compatibility. In particular, SiC CMP pads are becoming a fast-growing segment, supported by rising demand for SiC power devices in electric vehicles, renewable energy, industrial power systems, and 5G infrastructure. This segment has higher technical barriers and stronger growth potential than many conventional CMP pad applications. From the application perspective, semiconductor wafer polishing pads are mainly used in wafer fabrication, covering processes such as shallow trench isolation, interlayer dielectric polishing, metal interconnect polishing, barrier layer polishing, silicon wafer polishing, and compound semiconductor wafer polishing. As 8-inch and 12-inch wafers become mainstream and the industry moves toward larger wafer formats, pad dimensional stability, batch-to-batch consistency, and large-area polishing uniformity have become key competitive factors. Larger wafer sizes require better control of pad structure uniformity, surface morphology, and defect generation, making large-size pad development and stable mass production capabilities increasingly important. From the supply chain and manufacturing perspective, upstream materials include polyurethane resins, foaming materials, fillers, additives, substrates, and precision processing equipment. Midstream production involves formulation development, molding, foaming, curing, slicing, grooving, surface treatment, inspection, and clean packaging. Downstream customers include foundries, IDMs, memory manufacturers, and SiC power device manufacturers. The cost structure is mainly driven by raw materials, precision manufacturing, cleanroom production, quality inspection, R&D trials, and customer qualification. Single-line capacity is affected by molding equipment size, curing cycle, grooving efficiency, clean packaging capacity, and yield control. For high-end CMP pads, stable batch delivery and process consistency are more important than simple capacity expansion. The global CMP pad market remains concentrated among a limited number of suppliers with strong material formulation know-how, process experience, and long-term customer qualifications. Leading overseas players continue to hold advantages in advanced process nodes and major global customers. Chinese suppliers are accelerating market entry under the support of local wafer fab expansion, supply-chain security requirements, and domestic substitution policies, but high-end process qualification, batch stability, and multi-process compatibility remain key challenges. Looking forward, competition will increasingly focus on large-wafer compatibility, the balance between high removal rate and low defectivity, SiC and other

hard-to-polish materials, joint development with slurries, customer qualification capability, and global technical service support. Suppliers with strong material R&D, process understanding, scalable manufacturing, and customer penetration capabilities are expected to gain a stronger market position.

This report studies the global Semiconductor Wafer Polishing Pad production, demand, key manufacturers, and key regions.

This report is a detailed and comprehensive analysis of the world market for Semiconductor Wafer Polishing Pad and provides market size (US\$ million) and Year-over-Year (YoY) Growth, considering 2025 as the base year. This report explores demand trends and competition, as well as details the characteristics of Semiconductor Wafer Polishing Pad that contribute to its increasing demand across many markets.

Highlights and key features of the study

Global Semiconductor Wafer Polishing Pad total production and demand, 2021-2032, (K Pcs)

Global Semiconductor Wafer Polishing Pad total production value, 2021-2032, (USD Million)

Global Semiconductor Wafer Polishing Pad production by region & country, production, value, CAGR, 2021-2032, (USD Million) & (K Pcs), (based on production site)

Global Semiconductor Wafer Polishing Pad consumption by region & country, CAGR, 2021-2032 & (K Pcs)

U.S. VS China: Semiconductor Wafer Polishing Pad domestic production, consumption, key domestic manufacturers and share

Global Semiconductor Wafer Polishing Pad production by manufacturer, production, price, value and market share 2021-2026, (USD Million) & (K Pcs)

Global Semiconductor Wafer Polishing Pad production by Type, production, value, CAGR, 2021-2032, (USD Million) & (K Pcs)

Global Semiconductor Wafer Polishing Pad production by Application, production, value, CAGR, 2021-2032, (USD Million) & (K Pcs)

This report profiles key players in the global Semiconductor Wafer Polishing Pad market based on the following parameters - company overview, production, value, price, gross margin, product portfolio, geographical presence, and key developments. Key companies covered as a part of this study include Qnity, Entegris, Hubei Dinglong, Fujibo, IVT Technologies, SK enpulse, KPX Chemical, TWI Incorporated, 3M, FNS TECH, etc.

This report also provides key insights about market drivers, restraints, opportunities, new product launches or approvals.

Stakeholders would have ease in decision-making through various strategy matrices used in analyzing the World Semiconductor Wafer Polishing Pad market

Detailed Segmentation:

Each section contains quantitative market data including market by value (US\$ Millions), volume (production, consumption) & (K Pcs) and average price (US\$/Pcs) by manufacturer, by Type, and by Application. Data is given for the years 2021-2032 by year with 2025 as the base year, 2026 as the estimate year, and 2027-2032 as the forecast year.

Global Semiconductor Wafer Polishing Pad Market, By Region:

United States

China

Europe

Japan

South Korea

ASEAN

India

Rest of World

Global Semiconductor Wafer Polishing Pad Market, Segmentation by Type:

Polymer CMP Pad

Non-woven CMP Pad

Composite CMP Pad

Global Semiconductor Wafer Polishing Pad Market, Segmentation by Hardness:

Hard Pad

Soft Pad

Global Semiconductor Wafer Polishing Pad Market, Segmentation by Wafer Materials:

SiC Wafer

Si Wafer

Others

Global Semiconductor Wafer Polishing Pad Market, Segmentation by Application:

300 mm Wafer

200 mm Wafer

Others

Companies Profiled:

Qnity

Entegris

Hubei Dinglong

Fujibo

IVT Technologies

SK enpulse

KPX Chemical

TWI Incorporated

3M

FNS TECH

Key Questions Answered:

1. How big is the global Semiconductor Wafer Polishing Pad market?
2. What is the demand of the global Semiconductor Wafer Polishing Pad market?
3. What is the year over year growth of the global Semiconductor Wafer Polishing Pad market?
4. What is the production and production value of the global Semiconductor Wafer Polishing Pad market?
5. Who are the key producers in the global Semiconductor Wafer Polishing Pad market?
6. What are the growth factors driving the market demand?

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