

Global IC Packaging Design and Verification Supply, Demand and Key Producers, 2026-2032

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Abstracts

The global IC Packaging Design and Verification market size is expected to reach \$ 5216 million by 2032, rising at a market growth of 11.0% CAGR during the forecast period (2026-2032).

IC Packaging Design and Verification comprise specialized design automation tools, multiphysics simulation platforms, and professional engineering services used to plan, implement, optimize, and validate semiconductor packages and chip-to-system interconnect structures.

IC Packaging Design and Verification is evolving from a relatively narrow package-layout activity into a system-level engineering discipline that links semiconductor architecture, package integration, board design, manufacturing constraints, and end-product performance. In conventional packages, design work was primarily concerned with leadframe or substrate layout, wire-bond planning, package dimensions, and basic electrical or thermal checks. In chiplet-based, high-bandwidth-memory, 2.5D, 3D IC, hybrid-bonded, and co-packaged-optics architectures, package decisions directly affect bandwidth, latency, power delivery, thermal density, mechanical stress, warpage, yield, and system cost. Package analysis therefore needs to begin during architecture definition rather than after the silicon design has been completed. For market measurement purposes, the sector should be defined around identifiable software and engineering value, including package implementation, die and chiplet planning, chip-package-board co-design, physical verification, signal and power integrity, electromagnetic analysis, thermal and mechanical simulation, reliability assessment, and design signoff. It should not be measured by adding the full revenues of packaging manufacturers or semiconductor testing companies. Based on our research, the global narrow-scope market reached approximately USD 2.46 billion in 2025. Software

platforms represent the largest component, while project-based services supplied by OSATs, foundries, ASIC turnkey companies, and independent package-engineering specialists form a substantial second pillar. Comprehensive EDA suppliers control the principal design environments, whereas manufacturing-oriented providers contribute process knowledge, package characterization data, and design-to-production feedback that are difficult for software-only companies to replicate.

The global supply structure has two distinct layers. The first is a concentrated group of comprehensive EDA and multiphysics-platform providers. Cadence, Synopsys, and Siemens offer broad environments spanning package implementation, multi-die planning, physical verification, electrical analysis, and multiphysics signoff. Keysight, Zuken, Dassault Systèmes, and COMSOL maintain strong positions in RF and electromagnetic simulation, package-to-board co-design, or thermal and mechanical analysis. The second layer is substantially more fragmented and includes specialist electromagnetic and signal-integrity software companies, OSAT design centers, foundry enablement organizations, ASIC turnkey providers, contract research institutes, and regional package-engineering firms. Consolidation is strengthening the first layer: Synopsys completed its acquisition of Ansys in 2025, Siemens completed its acquisition of Altair, and Keysight has integrated ESI Group into its computer-aided-engineering portfolio. These transactions demonstrate that package verification is increasingly being combined with broader system simulation, digital engineering, and test-and-measurement environments. China is developing a parallel domestic supply base. Xpeedic offers chip-to-system SI, PI, electromagnetic, electrothermal, stress, and advanced-package capabilities; Empyrean has introduced package routing and package physical-verification products; and Zhuhai Silicon Chip Technology is developing a flow focused on 2.5D and 3D stacked-chip EDA. Domestic providers benefit from local support and customization, but still need broader foundry certifications, international production references, and validation on the largest heterogeneous-integration projects.

Demand growth is being led by artificial-intelligence accelerators, GPUs, custom data-center ASICs, high-bandwidth memory, and high-speed networking devices. These products use larger substrates, more dies, denser redistribution structures, and faster die-to-die and memory interfaces than conventional packages. As a result, power-delivery impedance, channel loss, crosstalk, thermal gradients, mechanical stress, warpage, and manufacturing yield must be analyzed as an interdependent system. Mobile and consumer electronics remain important markets for system-in-package, fan-out, and antenna-in-package design, although future growth will be driven more by RF complexity, millimeter-wave integration, and miniaturization than by unit-volume

expansion alone. Automotive demand is supported by centralized computing, advanced driver-assistance systems, power electronics, and functional-safety requirements, increasing the importance of thermal cycling, lifetime prediction, mechanical reliability, and traceable signoff flows. MEMS, medical, photonic, aerospace, and defense applications are smaller in revenue but often require customized structures, high-reliability qualification, and close engineering support, allowing specialist firms and research organizations to sustain attractive project economics. Foundries and OSATs are responding by expanding reference flows, package design rules, validated models, joint laboratories, and turnkey services. This shift brings design activity closer to process development and manufacturing, improves production-line utilization, and reduces the technical and schedule risks associated with introducing new advanced-package structures.

This report studies the global IC Packaging Design and Verification demand, key companies, and key regions.

This report is a detailed and comprehensive analysis of the world market for IC Packaging Design and Verification, and provides market size (US\$ million) and Year-over-Year (YoY) growth, considering 2025 as the base year. This report explores demand trends and competition, as well as details the characteristics of IC Packaging Design and Verification that contribute to its increasing demand across many markets.

Highlights and key features of the study

Global IC Packaging Design and Verification total market, 2021-2032, (USD Million)

Global IC Packaging Design and Verification total market by region & country, CAGR, 2021-2032, (USD Million)

U.S. VS China: IC Packaging Design and Verification total market, key domestic companies, and share, (USD Million)

Global IC Packaging Design and Verification revenue by player, revenue and market share 2021-2026, (USD Million)

Global IC Packaging Design and Verification total market by Type, CAGR, 2021-2032, (USD Million)

Global IC Packaging Design and Verification total market by Application, CAGR, 2021-2032, (USD Million)

This report profiles major players in the global IC Packaging Design and Verification market based on the following parameters - company overview, revenue, gross margin, product portfolio, geographical presence, and key developments. Key companies covered as a part of this study include Cadence Design Systems, Inc., Synopsys, Inc.,

Siemens AG, ASE Technology Holding Co., Ltd., Amkor Technology, Inc., Keysight Technologies, Inc., JCET Group Co., Ltd., Zuken Inc., TSMC, Samsung Electronics Co., Ltd., etc.

This report also provides key insights about market drivers, restraints, opportunities, new product launches or approvals.

Stakeholders would have ease in decision-making through various strategy matrices used in analyzing the world IC Packaging Design and Verification market

Detailed Segmentation:

Each section contains quantitative market data including market by value (US\$ Millions), by player, by regions, by Type, and by Application. Data is given for the years 2021-2032 by year with 2025 as the base year, 2026 as the estimate year, and 2027-2032 as the forecast year.

Global IC Packaging Design and Verification Market, By Region:

United States

China

Europe

Japan

South Korea

ASEAN

India

Rest of World

Global IC Packaging Design and Verification Market, Segmentation by Type:

Package Layout and Implementation Software

Co-design and System Planning Software

Others

Global IC Packaging Design and Verification Market, Segmentation by Package Architecture:

Conventional Leadframe

Wafer-Level and Fan-Out Packages

Others

Global IC Packaging Design and Verification Market, Segmentation by Verification Domain:

Physical Verification and DFM

Signal Integrity

Power Integrity

Others

Global IC Packaging Design and Verification Market, Segmentation by Application:

Data Center

Consumer Electronics

Communications

Others

Companies Profiled:

Cadence Design Systems, Inc.

Synopsys, Inc.

Siemens AG

ASE Technology Holding Co., Ltd.

Amkor Technology, Inc.

Keysight Technologies, Inc.

JCET Group Co., Ltd.

Zuken Inc.

TSMC

Samsung Electronics Co., Ltd.

Tongfu Microelectronics Co., Ltd.

Dassault Systèmes SE

Intel Corporation

Tianshui Huatian Technology Co., Ltd.

Xpeedic Technology, Inc.

Powertech Technology Inc.

Global Unichip Corporation

Alchip Technologies, Limited

COMSOL AB

Socionext Inc.

Chipbond Technology Corporation

NEPES Corporation

imec

Silicon Box Pte. Ltd.

Hana Micron Inc.

Fraunhofer IZM

VeriSilicon

SFA Semicon

Key Questions Answered

1. How big is the global IC Packaging Design and Verification market?
2. What is the demand of the global IC Packaging Design and Verification market?
3. What is the year over year growth of the global IC Packaging Design and Verification market?
4. What is the total value of the global IC Packaging Design and Verification market?
5. Who are the Major Players in the global IC Packaging Design and Verification market?
6. What are the growth factors driving the market demand?

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