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Global Chip Security Verification Software Market 2026 by Company, Regions, Type and Application, Forecast to 2032

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Abstracts

According to our (Global Info Research) latest study, the global Chip Security Verification Software market size was valued at US$ 319 million in 2025 and is forecast to a readjusted size of US$ 796 million by 2032 with a CAGR of 13.9% during review period.

Chip Security Verification Software refers to specialized software tools and software-centric platforms used to identify, analyze, verify, and document security weaknesses in semiconductor chips, systems-on-chip, processors, hardware IP, cryptographic implementations, and hardware–firmware interfaces. The market primarily covers EDA-integrated security verification modules, standalone verification software, security analysis workstation software, commercially supported open-source toolchains, and integrated test platforms in which proprietary software controls experiments and analyzes results. Core technical functions include formal security-property verification, secure access-path analysis, information-flow and taint tracking, simulation-based attack validation, side-channel leakage analysis, fault-injection analysis, security-coverage measurement, root-cause localization, and generation of auditable verification evidence. Chip Security Verification Software is applied across pre-silicon design, emulation and prototyping, post-silicon device evaluation, and cross-lifecycle verification workflows, supporting security validation for roots of trust, secure boot, access control, isolation mechanisms, cryptographic modules, debug and test interfaces, sensitive-data flows, and resistance to physical attacks.

Key Findings

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The confirmed core supplier pool contains 16 parent-company-level software and platform vendors

North America and Europe host 14 of the 16 confirmed core suppliers

Pre-silicon formal and information-flow verification forms the broadest commercial product group

Enterprise licensing and integrated platforms make shipment volume and ASP structurally non-comparable

Market Trends

Chip Security Verification Software is moving from predominantly post-silicon laboratory assessment toward earlier and more continuous verification across architecture, RTL, netlist, emulation, and physical-design stages. Formal security checking, information-flow tracking, and pre-silicon side-channel analysis increasingly aim to identify root causes before tape-out, when corrective design changes are less disruptive. Product development is also shifting from isolated vulnerability detection toward measurable security coverage, repeatable sign-off workflows, hardware–firmware co-verification, and traceable evidence that can be reused during product assurance and certification. Commercial tools now combine automated access-path verification, leakage localization, attack-scenario generation, and correlation between simulated and fabricated devices. This direction is reinforced by the increasing complexity of chiplets, AI accelerators, shared SoC resources, secure processors, and cryptographic implementations, which create security relationships that are difficult to assess through manual review or post-silicon testing alone. Official product portfolios from major EDA and device-security suppliers demonstrate the continued expansion of security verification into established semiconductor development workflows.

Market Dynamics

Drivers

Market demand is being driven by the rising economic and operational impact of hardware vulnerabilities, the increasing use of complex SoCs in connected and mission-critical systems, and the need to detect weaknesses before manufacturing. Security

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teams must evaluate isolation, access permissions, sensitive-data propagation, debug functions, cryptographic leakage, and resilience to voltage, clock, electromagnetic, and laser-based attacks. The 2025 CWE Most Important Hardware Weaknesses list highlights issues involving improper isolation of shared SoC resources, insecure debug and test interfaces, override of hardware locks, and insufficient protection against voltage and clock glitches, strengthening the case for systematic design-stage verification. Regulatory and product-assurance requirements are also increasing demand for structured, reproducible, and auditable security evidence.

Restraints

Adoption remains constrained by the specialist knowledge required to model hardware attack surfaces, define meaningful security properties, interpret formal results, and connect physical leakage or injected faults to their RTL-level causes. Enterprise EDA contracts frequently bundle security functions with broader simulation and formal-verification platforms, limiting revenue transparency and making purchasing decisions dependent on existing tool environments. Specialist platforms may also require integration with simulators, emulators, laboratory instruments, design databases, firmware environments, and certification processes. Long verification cycles, limited availability of experienced hardware-security engineers, and the cost of building representative attack models can delay deployment among smaller semiconductor companies. Internally developed tools and open-source frameworks further reduce the addressable commercial market for standardized products.

Opportunities

The strongest opportunities lie in shifting security analysis left into chip architecture and RTL development, extending verification from individual security blocks to complete SoCs, and connecting pre-silicon predictions with post-silicon measurements. Chiplet architectures, heterogeneous integration, RISC-V processors, AI accelerators, automotive domain controllers, hardware roots of trust, and post-quantum cryptographic implementations require scalable methods for validating permissions, isolation, data movement, and physical attack resistance. Opportunities also exist in automated mapping of design findings to hardware weakness taxonomies, generation of security-coverage metrics, and production of reusable assurance evidence. GlobalPlatform’s SESIP methodology supports structured component and platform evaluation and enables composition and reuse of security evidence, creating additional demand for tools that integrate verification results into repeatable assurance workflows.

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Challenges

The industry faces persistent challenges in standardizing product boundaries, verification metrics, license units, and the relationship between design verification, penetration testing, certification, and security consulting. A result generated by one tool may not be directly comparable with evidence generated through another methodology, particularly across formal verification, simulation, side-channel testing, and fault injection. False confidence is another risk: proving selected properties or detecting known weakness patterns does not demonstrate that a chip is free from all exploitable vulnerabilities. Vendors must continually update attack libraries, device models, verification engines, and integrations as architectures evolve. The market also remains exposed to consolidation, as larger EDA, semiconductor IP, and test-platform groups can acquire specialist capabilities and bundle them into broader product portfolios. Arteris completed its acquisition of Cycuity in January 2026, illustrating this integration trend.

Value Chain Analysis

The upstream layer of the Chip Security Verification Software value chain comprises formal-verification algorithms, simulation and emulation infrastructure, hardware-description languages, design databases, cloud and high-performance computing resources, vulnerability taxonomies, attack models, and interfaces to measurement or fault-injection instruments. These inputs determine verification capacity, scalability, coverage, and interoperability. High-value upstream capabilities are concentrated in formal engines, information-flow analysis, physical leakage modeling, automated root-cause localization, and reusable security-property libraries. Standards and weakness classifications also influence product development by defining the security evidence, vulnerability categories, and evaluation outputs expected by development and assurance teams.

The midstream layer consists of integrated EDA suppliers, independent security-verification software developers, commercially supported open-source tool providers, and software-centric test-platform companies. Value is created by converting complex attack models and verification techniques into repeatable engineering workflows, reducing manual analysis, locating vulnerabilities earlier, and producing evidence suitable for design reviews and assurance programs. Research and development, specialist engineering personnel, software maintenance, platform integration, and

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customer support represent the principal cost components. Standalone software and enterprise licenses offer software-oriented margin potential and recurring maintenance revenue, while integrated physical-test platforms carry higher hardware, laboratory, and application-support costs. The downstream value is realized by semiconductor and IP developers, security laboratories, device manufacturers, and system companies through reduced redesign risk, lower probability of certification failure, shorter security-debug cycles, and stronger evidence of product assurance.

Segment Insights

By product type, EDA-integrated security verification modules form the broadest commercial group because they can be deployed within established simulation, formal-verification, debug, and enterprise-license environments. Standalone security-verification software and security analysis workstations form a smaller but technically differentiated segment, particularly in information-flow verification, hardware weakness detection, side-channel analysis, and fault-injection assessment. Software-centric integrated test platforms remain important for post-silicon and cross-lifecycle workflows, while commercially supported open-source toolchains serve research, education, evaluation laboratories, and cost-sensitive engineering teams.

By verification stage, pre-silicon security verification represents the principal structured software opportunity, supported by formal property checking, secure-path verification, information-flow analysis, and simulation-based attack validation. Cross-lifecycle verification is emerging as an important growth direction because it links design-stage findings with measurements from fabricated devices. By core verification method, formal verification has the strongest integration with mainstream EDA workflows, while side-channel and fault-injection analysis retain higher specialist barriers. The most attractive application areas include root-of-trust and secure-boot verification, access-control and isolation analysis, sensitive-data-flow verification, cryptographic implementation security, debug-interface protection, and physical attack resistance.

Downstream Market Opportunities

Semiconductor and hardware IP development remains the central commercial application because security weaknesses introduced at architecture or RTL level can propagate across multiple products and customers. Automotive electronics, data-center and AI computing, aerospace and defense, payment and identity systems, secure elements, and connected industrial or consumer devices provide additional

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opportunities due to their reliance on protected execution, secure boot, cryptographic operations, trusted data movement, and long product lifecycles. Emerging demand is increasingly associated with systems that combine complex hardware with updateable firmware and third-party IP, where component-level assurance must be preserved after system integration. Regulatory preparation and reusable certification evidence can further increase adoption among companies supplying products with digital elements. The European Union's Cyber Resilience Act reporting obligations are scheduled to apply from September 11, 2026, while its principal product obligations will apply from December 11, 2027.

Regional Insights

North America represents the leading regional market and supply center for Chip Security Verification Software, supported by its concentration of major EDA platforms, semiconductor IP companies, specialist hardware-security software developers, AI and data-center chip programs, and aerospace and defense demand. Ten of the 16 confirmed core parent-company suppliers are headquartered in North America. The region has the strongest commercial position in formal security verification, information-flow analysis, static hardware-security sign-off, security test generation, and enterprise software integration.

Europe is the second major supply cluster, with particular strength in formal verification, side-channel analysis, fault-injection assessment, and structured security evaluation. Four confirmed core suppliers are headquartered in Europe, while France has developed a distinctive concentration of physical-attack and security-evaluation capabilities. The European regulatory and assurance environment is expected to support demand for traceable verification evidence. Asia-Pacific is the most important expansion opportunity: China has established local suppliers of software-driven chip-security test platforms, while Japan, South Korea, and Taiwan combine substantial semiconductor production and design activity with comparatively limited independent specialist software supply. GlobalPlatform has also reported initiatives aligning Taiwan's semiconductor ecosystem with SESIP requirements, supporting greater use of internationally reusable security-assurance evidence.

Competitive Landscape Analysis

The competitive landscape is structured around three supplier groups rather than a

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single uniform ranking. Large integrated EDA companies hold the strongest position in pre-silicon verification because their security applications operate inside widely adopted formal, simulation, debug, and sign-off environments. Scaled device-security and semiconductor-assurance platforms compete through broader coverage of information-flow analysis, side-channel assessment, fault injection, and correlation between design-stage and physical-device results. Specialized independent vendors differentiate through hardware-security sign-off, security test synthesis, automated weakness detection, processor-focused formal analysis, or lower-cost open toolchains. Competitive advantage depends less on license price alone than on verification capacity, attack-model depth, integration with established design environments, root-cause accuracy, measurable coverage, and the ability to produce auditable evidence. Market consolidation is likely to continue as EDA, system-IP, and electronic-test groups seek to add specialist security capabilities. The acquisition of Cycuity by Arteris demonstrates the strategic value of integrating semiconductor security assurance with broader SoC design and connectivity platforms, while the continued development of dedicated formal-security and pre-silicon leakage-analysis products indicates that security verification is becoming a more identifiable component of semiconductor engineering expenditure.

Report Scope

This report is a detailed and comprehensive analysis for global Chip Security Verification Software market. Both quantitative and qualitative analyses are presented by company, by region & country, by Type and by Application. As the market is constantly changing, this report explores the competition, supply and demand trends, as well as key factors that contribute to its changing demands across many markets. Company profiles and product examples of selected competitors, along with market share estimates of some of the selected leaders for the year 2025, are provided.

Key Features:

Global Chip Security Verification Software market size and forecasts, in consumption value ($ Million), 2021-2032

Global Chip Security Verification Software market size and forecasts by region and country, in consumption value ($ Million), 2021-2032

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Global Chip Security Verification Software market size and forecasts, by Type and by Application, in consumption value ($ Million), 2021-2032

Global Chip Security Verification Software market shares of main players, in revenue ($ Million), 2021-2026

The Primary Objectives in This Report Are:

To determine the size of the total market opportunity of global and key countries

To assess the growth potential for Chip Security Verification Software

To forecast future growth in each product and end-use market

To assess competitive factors affecting the marketplace

This report profiles key players in the global Chip Security Verification Software market based on the following parameters - company overview, revenue, gross margin, product portfolio, geographical presence, and key developments. Key companies covered as a part of this study include Siemens AG, Synopsys, Inc., Keysight Technologies, Inc., Cadence Design Systems, Inc., Rambus Inc., Arteris, Inc., Secure-IC S.A.S., Real Intent, Inc., eShard SAS, Breker Verification Systems, Inc., etc.

This report also provides key insights about market drivers, restraints, opportunities, new product launches or approvals.

Chip Security Verification Software market is split by Type and by Application. For the period 2021-2032, the growth among segments provides accurate calculations and forecasts for Consumption Value by Type and by Application. This analysis can help you expand your business by targeting qualified niche markets.

Market segmentation

Market segment by Type

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EDA-Integrated Security Verification Module

Standalone Security Verification Software

Security Analysis Workstation Software

Software-Centric Integrated Test Platform

Commercially Supported Open-Source Toolchain

Other

Market segment by Verification Stage

Pre-Silicon Security Verification

Cross-Lifecycle Security Verification

Other

Market segment by Core Verification Method

Formal Security Verification

Side-Channel Analysis

Fault-Injection Analysis

Other

Market segment by Deployment Model

Local Workstation Deployment

Private Cloud Deployment

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Public Cloud or SaaS Deployment

Other

Market segment by Application

Root of Trust and Secure Boot Verification

Access Control and Isolation Verification

Sensitive Data-Flow Verification

Cryptographic Security Verification

Debug and Test Interface Security Verification

Physical Attack Resistance Verification

Other

Market segment by players, this report covers

Siemens AG

Synopsys, Inc.

Keysight Technologies, Inc.

Cadence Design Systems, Inc.

Rambus Inc.

Arteris, Inc.

Secure-IC S.A.S.

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Real Intent, Inc.

eShard SAS

Breker Verification Systems, Inc.

FortifyIQ, Inc.

lowRISC C.I.C.

Caspia Technologies

Silicon Assurance

OSR

DPLS Lab

Market segment by regions, regional analysis covers

North America (United States, Canada and Mexico)

Europe (Germany, France, UK, Russia, Italy and Rest of Europe)

Asia-Pacific (China, Japan, South Korea, India, Southeast Asia and Rest of Asia-Pacific)

South America (Brazil, Rest of South America)

Middle East & Africa (Turkey, Saudi Arabia, UAE, Rest of Middle East & Africa)

Chapter Outline

Chapter 1, to describe Chip Security Verification Software product scope, market overview, market estimation caveats and base year.

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Chapter 2, to profile the top players of Chip Security Verification Software, with revenue, gross margin, and global market share of Chip Security Verification Software from 2021 to 2026.
Chapter 3, the Chip Security Verification Software competitive situation, revenue, and global market share of top players are analyzed emphatically by landscape contrast.
Chapter 4 and 5, to segment the market size by Type and by Application, with consumption value and growth rate by Type, by Application, from 2021 to 2032.
Chapter 6, 7, 8, 9, and 10, to break the market size data at the country level, with revenue and market share for key countries in the world, from 2021 to 2026.and Chip Security Verification Software market forecast, by regions, by Type and by Application, with consumption value, from 2027 to 2032.
Chapter 11, market dynamics, drivers, restraints, trends, Porters Five Forces analysis.
Chapter 12, the key raw materials and key suppliers, and industry chain of Chip Security Verification Software.
Chapter 13, to describe Chip Security Verification Software research findings and conclusion.

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