

Global 3D-Stacked Logic Chip Market 2026 by Manufacturers, Regions, Type and Application, Forecast to 2032

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Abstracts

According to our (Global Info Research) latest study, the global 3D-Stacked Logic Chip market size was valued at US\$ 6360 million in 2025 and is forecast to a readjusted size of US\$ 11571 million by 2032 with a CAGR of 7.5% during review period.

A 3D-stacked logic chip is a chip product centered on logic compute dies. It uses advanced packaging and three-dimensional integration technologies such as wafer-level stacking, die-level stacking, hybrid bonding, copper-to-copper direct bonding, TSVs, micro-bumps, redistribution layers, and silicon interposer collaboration to form high-density vertical interconnects among logic processing units, cache units, I/O units, interface units, or storage-coordination units. This type of chip is mainly used to address the bottlenecks of traditional large planar chips, including expanding die area, declining yield, longer interconnect distances, rising power consumption, and limited bandwidth. Its core value lies in shortening signal transmission paths, increasing die-to-die interconnect density, reducing energy consumption per unit of data transfer, and improving the bandwidth, latency, integration level, and performance density of computing systems. 3D-stacked logic chips are typically used in high-performance CPUs, GPUs, AI accelerators, data center processors, high-computing-power automotive chips, and complex SoCs, making them an important form of high-end logic chip driven jointly by advanced process nodes, chip architecture design, and advanced packaging.

3D-stacked logic chips represent one of the key paths for improving the performance of high-end logic chips. As the cost, yield, and power consumption pressures associated with continued advanced-node scaling continue to rise, the marginal benefits of improving performance solely through transistor size reduction are declining. By

vertically organizing functional dies such as compute, cache, I/O, and interface dies, 3D-stacked logic chips compress data paths that would otherwise require long-distance transmission across a two-dimensional plane into shorter three-dimensional interconnect structures, thereby increasing bandwidth, reducing latency, and lowering energy consumption per unit of data transfer. For AI accelerators, server processors, high-performance CPUs, GPUs, and complex SoCs, system performance bottlenecks no longer come only from the number of compute cores, but also from the efficiency of on-chip and die-to-die data movement. Against this backdrop, 3D-stacked logic chips are becoming an important technical direction for further improving the performance density of high-end computing chips.

The R&D and production of 3D-stacked logic chips represent a comprehensive competition involving advanced process nodes, chip architecture, bonding processes, thermal management, testing and validation, and package design capabilities. Technologies such as hybrid bonding, copper-to-copper direct bonding, TSVs, micro-bumps, and redistribution layers determine the interconnect density and signal transmission efficiency between dies, while post-stacking heat dissipation, stress control, yield management, and known-good-die screening directly affect whether products can enter large-scale production. Compared with traditional monolithic chip design, 3D-stacked logic chips require chip design companies, foundries, assembly and testing companies, and system customers to jointly define architecture and process requirements at an early stage, resulting in a higher threshold for supply chain collaboration.

From the demand side, 3D-stacked logic chips are first benefiting from AI computing and data center high-performance computing demand. Large model training, generative AI inference, cloud server upgrades, and high-bandwidth data processing are driving processors toward higher computing power, larger caches, wider I/O, and lower latency. Traditional planar chips and conventional multi-chip packages are unlikely to meet these system-level requirements over the long term. As high-end computing chip customers continue to raise requirements for energy efficiency, bandwidth, and package footprint, 3D-stacked logic chips are expected to gradually expand from a limited number of flagship processors and high-end accelerator chips into server CPUs, edge AI chips, high-computing-power automotive chips, and customized SoCs.

This report is a detailed and comprehensive analysis for global 3D-Stacked Logic Chip market. Both quantitative and qualitative analyses are presented by manufacturers, by region & country, by Stacking Object and by Application. As the market is constantly changing, this report explores the competition, supply and demand trends, as well as

key factors that contribute to its changing demands across many markets. Company profiles and product examples of selected competitors, along with market share estimates of some of the selected leaders for the year 2025, are provided.

Key Features:

Global 3D-Stacked Logic Chip market size and forecasts, in consumption value (\$ Million), sales quantity (Million Units), and average selling prices (US\$/Unit), 2021-2032

Global 3D-Stacked Logic Chip market size and forecasts by region and country, in consumption value (\$ Million), sales quantity (Million Units), and average selling prices (US\$/Unit), 2021-2032

Global 3D-Stacked Logic Chip market size and forecasts, by Stacking Object and by Application, in consumption value (\$ Million), sales quantity (Million Units), and average selling prices (US\$/Unit), 2021-2032

Global 3D-Stacked Logic Chip market shares of main players, shipments in revenue (\$ Million), sales quantity (Million Units), and ASP (US\$/Unit), 2021-2026

The Primary Objectives in This Report Are:

- To determine the size of the total market opportunity of global and key countries

- To assess the growth potential for 3D-Stacked Logic Chip

- To forecast future growth in each product and end-use market

- To assess competitive factors affecting the marketplace

This report profiles key players in the global 3D-Stacked Logic Chip market based on the following parameters - company overview, sales quantity, revenue, price, gross margin, product portfolio, geographical presence, and key developments. Key companies covered as a part of this study include TSMC, Intel, Samsung Electronics, AMD, ASE Technology Holding, Amkor Technology, JCET Group, Tongfu Microelectronics, Socionext, GlobalFoundries, etc.

This report also provides key insights about market drivers, restraints, opportunities,

new product launches or approvals.

Market Segmentation

3D-Stacked Logic Chip market is split by Stacking Object and by Application. For the period 2021-2032, the growth among segments provides accurate calculations and forecasts for consumption value by Stacking Object, and by Application in terms of volume and value. This analysis can help you expand your business by targeting qualified niche markets.

Market segment by Stacking Object

Logic-to-Logic Stacked Chip

Logic-to-Cache Stacked Chip

Logic-to-I/O Stacked Chip

Logic-to-Interface Stacked Chip

Logic-to-Memory Co-Stacked Chip

Market segment by Bonding Method

Hybrid Bonding Chip

Micro-Bump Bonding Chip

Cu-Cu Direct Bonding Chip

Wafer Bonding Chip

Other

Market segment by Interconnect Structure

TSV Interconnect Chip

TSV-Less Direct Interconnect Chip

Silicon Interposer-Assisted Chip

Other

Market segment by Application

Cloud Computing Vendor

Server Vendor

Chip Design Company

Automotive Electronics Vendor

Telecommunications Equipment Vendor

Major players covered

TSMC

Intel

Samsung Electronics

AMD

ASE Technology Holding

Amkor Technology

JCET Group

Tongfu Microelectronics

Socionext

GlobalFoundries

Market segment by region, regional analysis covers

North America (United States, Canada, and Mexico)

Europe (Germany, France, United Kingdom, Russia, Italy, and Rest of Europe)

Asia-Pacific (China, Japan, Korea, India, Southeast Asia, and Australia)

South America (Brazil, Argentina, Colombia, and Rest of South America)

Middle East & Africa (Saudi Arabia, UAE, Egypt, South Africa, and Rest of Middle East & Africa)

The content of the study subjects, includes a total of 15 chapters:

Chapter 1, to describe 3D-Stacked Logic Chip product scope, market overview, market estimation caveats and base year.

Chapter 2, to profile the top manufacturers of 3D-Stacked Logic Chip, with price, sales quantity, revenue, and global market share of 3D-Stacked Logic Chip from 2021 to 2026.

Chapter 3, the 3D-Stacked Logic Chip competitive situation, sales quantity, revenue, and global market share of top manufacturers are analyzed emphatically by landscape contrast.

Chapter 4, the 3D-Stacked Logic Chip breakdown data are shown at the regional level, to show the sales quantity, consumption value, and growth by regions, from 2021 to 2032.

Chapter 5 and 6, to segment the sales by Stacking Object and by Application, with sales market share and growth rate by Stacking Object, by Application, from 2021 to 2032.

Chapter 7, 8, 9, 10 and 11, to break the sales data at the country level, with sales quantity, consumption value, and market share for key countries in the world, from 2021 to 2026. and 3D-Stacked Logic Chip market forecast, by regions, by Stacking Object, and by Application, with sales and revenue, from 2027 to 2032.

Chapter 12, market dynamics, drivers, restraints, trends, and Porters Five Forces analysis.

Chapter 13, the key raw materials and key suppliers, and industry chain of 3D-Stacked Logic Chip.

Chapter 14 and 15, to describe 3D-Stacked Logic Chip sales channel, distributors, customers, research findings and conclusion.

Contents

1 MARKET OVERVIEW

1.1 Product Overview and Scope

1.2 Market Estimation Caveats and Base Year

1.3 Market Analysis by Stacking Object

1.3.1 Overview: Global 3D-Stacked Logic Chip Consumption Value by Stacking Object: 2021 Versus 2025 Versus 2032

1.3.2 Logic-to-Logic Stacked Chip

1.3.3 Logic-to-Cache Stacked Chip

1.3.4 Logic-to-I/O Stacked Chip

1.3.5 Logic-to-Interface Stacked Chip

1.3.6 Logic-to-Memory Co-Stacked Chip

1.4 Market Analysis by Bonding Method

1.4.1 Overview: Global 3D-Stacked Logic Chip Consumption Value by Bonding Method: 2021 Versus 2025 Versus 2032

1.4.2 Hybrid Bonding Chip

1.4.3 Micro-Bump Bonding Chip

1.4.4 Cu-Cu Direct Bonding Chip

1.4.5 Wafer Bonding Chip

1.4.6 Other

1.5 Market Analysis by Interconnect Structure

1.5.1 Overview: Global 3D-Stacked Logic Chip Consumption Value by Interconnect Structure: 2021 Versus 2025 Versus 2032

1.5.2 TSV Interconnect Chip

1.5.3 TSV-Less Direct Interconnect Chip

1.5.4 Silicon Interposer-Assisted Chip

1.5.5 Other

1.6 Market Analysis by Application

1.6.1 Overview: Global 3D-Stacked Logic Chip Consumption Value by Application: 2021 Versus 2025 Versus 2032

1.6.2 Cloud Computing Vendor

1.6.3 Server Vendor

1.6.4 Chip Design Company

1.6.5 Automotive Electronics Vendor

1.6.6 Telecommunications Equipment Vendor

1.7 Global 3D-Stacked Logic Chip Market Size & Forecast

1.7.1 Global 3D-Stacked Logic Chip Consumption Value (2021 & 2025 & 2032)

1.7.2 Global 3D-Stacked Logic Chip Sales Quantity (2021-2032)

1.7.3 Global 3D-Stacked Logic Chip Average Price (2021-2032)

2 MANUFACTURERS PROFILES

2.1 TSMC

2.1.1 TSMC Details

2.1.2 TSMC Major Business

2.1.3 TSMC 3D-Stacked Logic Chip Product and Services

2.1.4 TSMC 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)

2.1.5 TSMC Recent Developments/Updates

2.2 Intel

2.2.1 Intel Details

2.2.2 Intel Major Business

2.2.3 Intel 3D-Stacked Logic Chip Product and Services

2.2.4 Intel 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)

2.2.5 Intel Recent Developments/Updates

2.3 Samsung Electronics

2.3.1 Samsung Electronics Details

2.3.2 Samsung Electronics Major Business

2.3.3 Samsung Electronics 3D-Stacked Logic Chip Product and Services

2.3.4 Samsung Electronics 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)

2.3.5 Samsung Electronics Recent Developments/Updates

2.4 AMD

2.4.1 AMD Details

2.4.2 AMD Major Business

2.4.3 AMD 3D-Stacked Logic Chip Product and Services

2.4.4 AMD 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)

2.4.5 AMD Recent Developments/Updates

2.5 ASE Technology Holding

2.5.1 ASE Technology Holding Details

2.5.2 ASE Technology Holding Major Business

2.5.3 ASE Technology Holding 3D-Stacked Logic Chip Product and Services

2.5.4 ASE Technology Holding 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)

- 2.5.5 ASE Technology Holding Recent Developments/Updates
- 2.6 Amkor Technology
 - 2.6.1 Amkor Technology Details
 - 2.6.2 Amkor Technology Major Business
 - 2.6.3 Amkor Technology 3D-Stacked Logic Chip Product and Services
 - 2.6.4 Amkor Technology 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)
 - 2.6.5 Amkor Technology Recent Developments/Updates
- 2.7 JCET Group
 - 2.7.1 JCET Group Details
 - 2.7.2 JCET Group Major Business
 - 2.7.3 JCET Group 3D-Stacked Logic Chip Product and Services
 - 2.7.4 JCET Group 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)
 - 2.7.5 JCET Group Recent Developments/Updates
- 2.8 Tongfu Microelectronics
 - 2.8.1 Tongfu Microelectronics Details
 - 2.8.2 Tongfu Microelectronics Major Business
 - 2.8.3 Tongfu Microelectronics 3D-Stacked Logic Chip Product and Services
 - 2.8.4 Tongfu Microelectronics 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)
 - 2.8.5 Tongfu Microelectronics Recent Developments/Updates
- 2.9 Socionext
 - 2.9.1 Socionext Details
 - 2.9.2 Socionext Major Business
 - 2.9.3 Socionext 3D-Stacked Logic Chip Product and Services
 - 2.9.4 Socionext 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)
 - 2.9.5 Socionext Recent Developments/Updates
- 2.10 GlobalFoundries
 - 2.10.1 GlobalFoundries Details
 - 2.10.2 GlobalFoundries Major Business
 - 2.10.3 GlobalFoundries 3D-Stacked Logic Chip Product and Services
 - 2.10.4 GlobalFoundries 3D-Stacked Logic Chip Sales Quantity, Average Price, Revenue, Gross Margin and Market Share (2021-2026)
 - 2.10.5 GlobalFoundries Recent Developments/Updates

3 COMPETITIVE ENVIRONMENT: 3D-STACKED LOGIC CHIP BY MANUFACTURER

- 3.1 Global 3D-Stacked Logic Chip Sales Quantity by Manufacturer (2021-2026)
- 3.2 Global 3D-Stacked Logic Chip Revenue by Manufacturer (2021-2026)
- 3.3 Global 3D-Stacked Logic Chip Average Price by Manufacturer (2021-2026)
- 3.4 Market Share Analysis (2025)
 - 3.4.1 Producer Shipments of 3D-Stacked Logic Chip by Manufacturer Revenue (\$MM) and Market Share (%): 2025
 - 3.4.2 Top 3 3D-Stacked Logic Chip Manufacturer Market Share in 2025
 - 3.4.3 Top 6 3D-Stacked Logic Chip Manufacturer Market Share in 2025
- 3.5 3D-Stacked Logic Chip Market: Overall Company Footprint Analysis
 - 3.5.1 3D-Stacked Logic Chip Market: Region Footprint
 - 3.5.2 3D-Stacked Logic Chip Market: Company Product Type Footprint
 - 3.5.3 3D-Stacked Logic Chip Market: Company Product Application Footprint
- 3.6 New Market Entrants and Barriers to Market Entry
- 3.7 Mergers, Acquisition, Agreements, and Collaborations

4 CONSUMPTION ANALYSIS BY REGION

- 4.1 Global 3D-Stacked Logic Chip Market Size by Region
 - 4.1.1 Global 3D-Stacked Logic Chip Sales Quantity by Region (2021-2032)
 - 4.1.2 Global 3D-Stacked Logic Chip Consumption Value by Region (2021-2032)
 - 4.1.3 Global 3D-Stacked Logic Chip Average Price by Region (2021-2032)
- 4.2 North America 3D-Stacked Logic Chip Consumption Value (2021-2032)
- 4.3 Europe 3D-Stacked Logic Chip Consumption Value (2021-2032)
- 4.4 Asia-Pacific 3D-Stacked Logic Chip Consumption Value (2021-2032)
- 4.5 South America 3D-Stacked Logic Chip Consumption Value (2021-2032)
- 4.6 Middle East & Africa 3D-Stacked Logic Chip Consumption Value (2021-2032)

5 MARKET SEGMENT BY STACKING OBJECT

- 5.1 Global 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2032)
- 5.2 Global 3D-Stacked Logic Chip Consumption Value by Stacking Object (2021-2032)
- 5.3 Global 3D-Stacked Logic Chip Average Price by Stacking Object (2021-2032)

6 MARKET SEGMENT BY APPLICATION

- 6.1 Global 3D-Stacked Logic Chip Sales Quantity by Application (2021-2032)
- 6.2 Global 3D-Stacked Logic Chip Consumption Value by Application (2021-2032)
- 6.3 Global 3D-Stacked Logic Chip Average Price by Application (2021-2032)

7 NORTH AMERICA

7.1 North America 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2032)

7.2 North America 3D-Stacked Logic Chip Sales Quantity by Application (2021-2032)

7.3 North America 3D-Stacked Logic Chip Market Size by Country

7.3.1 North America 3D-Stacked Logic Chip Sales Quantity by Country (2021-2032)

7.3.2 North America 3D-Stacked Logic Chip Consumption Value by Country (2021-2032)

7.3.3 United States Market Size and Forecast (2021-2032)

7.3.4 Canada Market Size and Forecast (2021-2032)

7.3.5 Mexico Market Size and Forecast (2021-2032)

8 EUROPE

8.1 Europe 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2032)

8.2 Europe 3D-Stacked Logic Chip Sales Quantity by Application (2021-2032)

8.3 Europe 3D-Stacked Logic Chip Market Size by Country

8.3.1 Europe 3D-Stacked Logic Chip Sales Quantity by Country (2021-2032)

8.3.2 Europe 3D-Stacked Logic Chip Consumption Value by Country (2021-2032)

8.3.3 Germany Market Size and Forecast (2021-2032)

8.3.4 France Market Size and Forecast (2021-2032)

8.3.5 United Kingdom Market Size and Forecast (2021-2032)

8.3.6 Russia Market Size and Forecast (2021-2032)

8.3.7 Italy Market Size and Forecast (2021-2032)

9 ASIA-PACIFIC

9.1 Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2032)

9.2 Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Application (2021-2032)

9.3 Asia-Pacific 3D-Stacked Logic Chip Market Size by Region

9.3.1 Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Region (2021-2032)

9.3.2 Asia-Pacific 3D-Stacked Logic Chip Consumption Value by Region (2021-2032)

9.3.3 China Market Size and Forecast (2021-2032)

9.3.4 Japan Market Size and Forecast (2021-2032)

9.3.5 South Korea Market Size and Forecast (2021-2032)

9.3.6 India Market Size and Forecast (2021-2032)

9.3.7 Southeast Asia Market Size and Forecast (2021-2032)

9.3.8 Australia Market Size and Forecast (2021-2032)

10 SOUTH AMERICA

- 10.1 South America 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2032)
- 10.2 South America 3D-Stacked Logic Chip Sales Quantity by Application (2021-2032)
- 10.3 South America 3D-Stacked Logic Chip Market Size by Country
 - 10.3.1 South America 3D-Stacked Logic Chip Sales Quantity by Country (2021-2032)
 - 10.3.2 South America 3D-Stacked Logic Chip Consumption Value by Country (2021-2032)
 - 10.3.3 Brazil Market Size and Forecast (2021-2032)
 - 10.3.4 Argentina Market Size and Forecast (2021-2032)

11 MIDDLE EAST & AFRICA

- 11.1 Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2032)
- 11.2 Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Application (2021-2032)
- 11.3 Middle East & Africa 3D-Stacked Logic Chip Market Size by Country
 - 11.3.1 Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Country (2021-2032)
 - 11.3.2 Middle East & Africa 3D-Stacked Logic Chip Consumption Value by Country (2021-2032)
 - 11.3.3 Turkey Market Size and Forecast (2021-2032)
 - 11.3.4 Egypt Market Size and Forecast (2021-2032)
 - 11.3.5 Saudi Arabia Market Size and Forecast (2021-2032)
 - 11.3.6 South Africa Market Size and Forecast (2021-2032)

12 MARKET DYNAMICS

- 12.1 3D-Stacked Logic Chip Market Drivers
- 12.2 3D-Stacked Logic Chip Market Restraints
- 12.3 3D-Stacked Logic Chip Trends Analysis
- 12.4 Porters Five Forces Analysis
 - 12.4.1 Threat of New Entrants
 - 12.4.2 Bargaining Power of Suppliers
 - 12.4.3 Bargaining Power of Buyers
 - 12.4.4 Threat of Substitutes

12.4.5 Competitive Rivalry

13 RAW MATERIAL AND INDUSTRY CHAIN

13.1 Raw Material of 3D-Stacked Logic Chip and Key Manufacturers

13.2 Manufacturing Costs Percentage of 3D-Stacked Logic Chip

13.3 3D-Stacked Logic Chip Production Process

13.4 Industry Value Chain Analysis

14 SHIPMENTS BY DISTRIBUTION CHANNEL

14.1 Sales Channel

14.1.1 Direct to End-User

14.1.2 Distributors

14.2 3D-Stacked Logic Chip Typical Distributors

14.3 3D-Stacked Logic Chip Typical Customers

15 RESEARCH FINDINGS AND CONCLUSION

16 APPENDIX

16.1 Methodology

16.2 Research Process and Data Source

16.3 Disclaimer

List Of Tables

LIST OF TABLES

Table 1. Global 3D-Stacked Logic Chip Consumption Value by Stacking Object, (USD Million), 2021 & 2025 & 2032

Table 2. Global 3D-Stacked Logic Chip Consumption Value by Bonding Method, (USD Million), 2021 & 2025 & 2032

Table 3. Global 3D-Stacked Logic Chip Consumption Value by Interconnect Structure, (USD Million), 2021 & 2025 & 2032

Table 4. Global 3D-Stacked Logic Chip Consumption Value by Application, (USD Million), 2021 & 2025 & 2032

Table 5. TSMC Basic Information, Manufacturing Base and Competitors

Table 6. TSMC Major Business

Table 7. TSMC 3D-Stacked Logic Chip Product and Services

Table 8. TSMC 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 9. TSMC Recent Developments/Updates

Table 10. Intel Basic Information, Manufacturing Base and Competitors

Table 11. Intel Major Business

Table 12. Intel 3D-Stacked Logic Chip Product and Services

Table 13. Intel 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 14. Intel Recent Developments/Updates

Table 15. Samsung Electronics Basic Information, Manufacturing Base and Competitors

Table 16. Samsung Electronics Major Business

Table 17. Samsung Electronics 3D-Stacked Logic Chip Product and Services

Table 18. Samsung Electronics 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 19. Samsung Electronics Recent Developments/Updates

Table 20. AMD Basic Information, Manufacturing Base and Competitors

Table 21. AMD Major Business

Table 22. AMD 3D-Stacked Logic Chip Product and Services

Table 23. AMD 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 24. AMD Recent Developments/Updates

Table 25. ASE Technology Holding Basic Information, Manufacturing Base and Competitors

Table 26. ASE Technology Holding Major Business

Table 27. ASE Technology Holding 3D-Stacked Logic Chip Product and Services

Table 28. ASE Technology Holding 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 29. ASE Technology Holding Recent Developments/Updates

Table 30. Amkor Technology Basic Information, Manufacturing Base and Competitors

Table 31. Amkor Technology Major Business

Table 32. Amkor Technology 3D-Stacked Logic Chip Product and Services

Table 33. Amkor Technology 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 34. Amkor Technology Recent Developments/Updates

Table 35. JCET Group Basic Information, Manufacturing Base and Competitors

Table 36. JCET Group Major Business

Table 37. JCET Group 3D-Stacked Logic Chip Product and Services

Table 38. JCET Group 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 39. JCET Group Recent Developments/Updates

Table 40. Tongfu Microelectronics Basic Information, Manufacturing Base and Competitors

Table 41. Tongfu Microelectronics Major Business

Table 42. Tongfu Microelectronics 3D-Stacked Logic Chip Product and Services

Table 43. Tongfu Microelectronics 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 44. Tongfu Microelectronics Recent Developments/Updates

Table 45. Socionext Basic Information, Manufacturing Base and Competitors

Table 46. Socionext Major Business

Table 47. Socionext 3D-Stacked Logic Chip Product and Services

Table 48. Socionext 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 49. Socionext Recent Developments/Updates

Table 50. GlobalFoundries Basic Information, Manufacturing Base and Competitors

Table 51. GlobalFoundries Major Business

Table 52. GlobalFoundries 3D-Stacked Logic Chip Product and Services

Table 53. GlobalFoundries 3D-Stacked Logic Chip Sales Quantity (Million Units), Average Price (US\$/Unit), Revenue (USD Million), Gross Margin and Market Share (2021-2026)

Table 54. GlobalFoundries Recent Developments/Updates

Table 55. Global 3D-Stacked Logic Chip Sales Quantity by Manufacturer (2021-2026) & (Million Units)

Table 56. Global 3D-Stacked Logic Chip Revenue by Manufacturer (2021-2026) & (USD Million)

Table 57. Global 3D-Stacked Logic Chip Average Price by Manufacturer (2021-2026) & (US\$/Unit)

Table 58. Market Position of Manufacturers in 3D-Stacked Logic Chip, (Tier 1, Tier 2, and Tier 3), Based on Revenue in 2025

Table 59. Head Office and 3D-Stacked Logic Chip Production Site of Key Manufacturer

Table 60. 3D-Stacked Logic Chip Market: Company Product Type Footprint

Table 61. 3D-Stacked Logic Chip Market: Company Product Application Footprint

Table 62. 3D-Stacked Logic Chip New Market Entrants and Barriers to Market Entry

Table 63. 3D-Stacked Logic Chip Mergers, Acquisition, Agreements, and Collaborations

Table 64. Global 3D-Stacked Logic Chip Consumption Value by Region (2021-2025-2032) & (USD Million) & CAGR

Table 65. Global 3D-Stacked Logic Chip Sales Quantity by Region (2021-2026) & (Million Units)

Table 66. Global 3D-Stacked Logic Chip Sales Quantity by Region (2027-2032) & (Million Units)

Table 67. Global 3D-Stacked Logic Chip Consumption Value by Region (2021-2026) & (USD Million)

Table 68. Global 3D-Stacked Logic Chip Consumption Value by Region (2027-2032) & (USD Million)

Table 69. Global 3D-Stacked Logic Chip Average Price by Region (2021-2026) & (US\$/Unit)

Table 70. Global 3D-Stacked Logic Chip Average Price by Region (2027-2032) & (US\$/Unit)

Table 71. Global 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2026) & (Million Units)

Table 72. Global 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2027-2032) & (Million Units)

Table 73. Global 3D-Stacked Logic Chip Consumption Value by Stacking Object (2021-2026) & (USD Million)

Table 74. Global 3D-Stacked Logic Chip Consumption Value by Stacking Object (2027-2032) & (USD Million)

Table 75. Global 3D-Stacked Logic Chip Average Price by Stacking Object (2021-2026) & (US\$/Unit)

Table 76. Global 3D-Stacked Logic Chip Average Price by Stacking Object (2027-2032)

& (US\$/Unit)

Table 77. Global 3D-Stacked Logic Chip Sales Quantity by Application (2021-2026) & (Million Units)

Table 78. Global 3D-Stacked Logic Chip Sales Quantity by Application (2027-2032) & (Million Units)

Table 79. Global 3D-Stacked Logic Chip Consumption Value by Application (2021-2026) & (USD Million)

Table 80. Global 3D-Stacked Logic Chip Consumption Value by Application (2027-2032) & (USD Million)

Table 81. Global 3D-Stacked Logic Chip Average Price by Application (2021-2026) & (US\$/Unit)

Table 82. Global 3D-Stacked Logic Chip Average Price by Application (2027-2032) & (US\$/Unit)

Table 83. North America 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2026) & (Million Units)

Table 84. North America 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2027-2032) & (Million Units)

Table 85. North America 3D-Stacked Logic Chip Sales Quantity by Application (2021-2026) & (Million Units)

Table 86. North America 3D-Stacked Logic Chip Sales Quantity by Application (2027-2032) & (Million Units)

Table 87. North America 3D-Stacked Logic Chip Sales Quantity by Country (2021-2026) & (Million Units)

Table 88. North America 3D-Stacked Logic Chip Sales Quantity by Country (2027-2032) & (Million Units)

Table 89. North America 3D-Stacked Logic Chip Consumption Value by Country (2021-2026) & (USD Million)

Table 90. North America 3D-Stacked Logic Chip Consumption Value by Country (2027-2032) & (USD Million)

Table 91. Europe 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2026) & (Million Units)

Table 92. Europe 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2027-2032) & (Million Units)

Table 93. Europe 3D-Stacked Logic Chip Sales Quantity by Application (2021-2026) & (Million Units)

Table 94. Europe 3D-Stacked Logic Chip Sales Quantity by Application (2027-2032) & (Million Units)

Table 95. Europe 3D-Stacked Logic Chip Sales Quantity by Country (2021-2026) & (Million Units)

Table 96. Europe 3D-Stacked Logic Chip Sales Quantity by Country (2027-2032) & (Million Units)

Table 97. Europe 3D-Stacked Logic Chip Consumption Value by Country (2021-2026) & (USD Million)

Table 98. Europe 3D-Stacked Logic Chip Consumption Value by Country (2027-2032) & (USD Million)

Table 99. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2026) & (Million Units)

Table 100. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2027-2032) & (Million Units)

Table 101. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Application (2021-2026) & (Million Units)

Table 102. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Application (2027-2032) & (Million Units)

Table 103. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Region (2021-2026) & (Million Units)

Table 104. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity by Region (2027-2032) & (Million Units)

Table 105. Asia-Pacific 3D-Stacked Logic Chip Consumption Value by Region (2021-2026) & (USD Million)

Table 106. Asia-Pacific 3D-Stacked Logic Chip Consumption Value by Region (2027-2032) & (USD Million)

Table 107. South America 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2021-2026) & (Million Units)

Table 108. South America 3D-Stacked Logic Chip Sales Quantity by Stacking Object (2027-2032) & (Million Units)

Table 109. South America 3D-Stacked Logic Chip Sales Quantity by Application (2021-2026) & (Million Units)

Table 110. South America 3D-Stacked Logic Chip Sales Quantity by Application (2027-2032) & (Million Units)

Table 111. South America 3D-Stacked Logic Chip Sales Quantity by Country (2021-2026) & (Million Units)

Table 112. South America 3D-Stacked Logic Chip Sales Quantity by Country (2027-2032) & (Million Units)

Table 113. South America 3D-Stacked Logic Chip Consumption Value by Country (2021-2026) & (USD Million)

Table 114. South America 3D-Stacked Logic Chip Consumption Value by Country (2027-2032) & (USD Million)

Table 115. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Stacking

Object (2021-2026) & (Million Units)

Table 116. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Stacking
Object (2027-2032) & (Million Units)

Table 117. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Application
(2021-2026) & (Million Units)

Table 118. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Application
(2027-2032) & (Million Units)

Table 119. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Country
(2021-2026) & (Million Units)

Table 120. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity by Country
(2027-2032) & (Million Units)

Table 121. Middle East & Africa 3D-Stacked Logic Chip Consumption Value by Country
(2021-2026) & (USD Million)

Table 122. Middle East & Africa 3D-Stacked Logic Chip Consumption Value by Country
(2027-2032) & (USD Million)

Table 123. 3D-Stacked Logic Chip Raw Material

Table 124. Key Manufacturers of 3D-Stacked Logic Chip Raw Materials

Table 125. 3D-Stacked Logic Chip Typical Distributors

Table 126. 3D-Stacked Logic Chip Typical Customers

List Of Figures

LIST OF FIGURES

Figure 1. 3D-Stacked Logic Chip Picture

Figure 2. Global 3D-Stacked Logic Chip Revenue by Stacking Object, (USD Million), 2021 & 2025 & 2032

Figure 3. Global 3D-Stacked Logic Chip Revenue Market Share by Stacking Object in 2025

Figure 4. Logic-to-Logic Stacked Chip Examples

Figure 5. Logic-to-Cache Stacked Chip Examples

Figure 6. Logic-to-I/O Stacked Chip Examples

Figure 7. Logic-to-Interface Stacked Chip Examples

Figure 8. Logic-to-Memory Co-Stacked Chip Examples

Figure 9. Global 3D-Stacked Logic Chip Revenue by Bonding Method, (USD Million), 2021 & 2025 & 2032

Figure 10. Global 3D-Stacked Logic Chip Revenue Market Share by Bonding Method in 2025

Figure 11. Hybrid Bonding Chip Examples

Figure 12. Micro-Bump Bonding Chip Examples

Figure 13. Cu-Cu Direct Bonding Chip Examples

Figure 14. Wafer Bonding Chip Examples

Figure 15. Other Examples

Figure 16. Global 3D-Stacked Logic Chip Revenue by Interconnect Structure, (USD Million), 2021 & 2025 & 2032

Figure 17. Global 3D-Stacked Logic Chip Revenue Market Share by Interconnect Structure in 2025

Figure 18. TSV Interconnect Chip Examples

Figure 19. TSV-Less Direct Interconnect Chip Examples

Figure 20. Silicon Interposer-Assisted Chip Examples

Figure 21. Other Examples

Figure 22. Global 3D-Stacked Logic Chip Consumption Value by Application, (USD Million), 2021 & 2025 & 2032

Figure 23. Global 3D-Stacked Logic Chip Revenue Market Share by Application in 2025

Figure 24. Cloud Computing Vendor Examples

Figure 25. Server Vendor Examples

Figure 26. Chip Design Company Examples

Figure 27. Automotive Electronics Vendor Examples

Figure 28. Telecommunications Equipment Vendor Examples

Figure 29. Global 3D-Stacked Logic Chip Consumption Value, (USD Million): 2021 & 2025 & 2032

Figure 30. Global 3D-Stacked Logic Chip Consumption Value and Forecast (2021-2032) & (USD Million)

Figure 31. Global 3D-Stacked Logic Chip Sales Quantity (2021-2032) & (Million Units)

Figure 32. Global 3D-Stacked Logic Chip Price (2021-2032) & (US\$/Unit)

Figure 33. Global 3D-Stacked Logic Chip Sales Quantity Market Share by Manufacturer in 2025

Figure 34. Global 3D-Stacked Logic Chip Revenue Market Share by Manufacturer in 2025

Figure 35. Producer Shipments of 3D-Stacked Logic Chip by Manufacturer Sales (\$MM) and Market Share (%): 2025

Figure 36. Top 3 3D-Stacked Logic Chip Manufacturer (Revenue) Market Share in 2025

Figure 37. Top 6 3D-Stacked Logic Chip Manufacturer (Revenue) Market Share in 2025

Figure 38. Global 3D-Stacked Logic Chip Sales Quantity Market Share by Region (2021-2032)

Figure 39. Global 3D-Stacked Logic Chip Consumption Value Market Share by Region (2021-2032)

Figure 40. North America 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 41. Europe 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 42. Asia-Pacific 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 43. South America 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 44. Middle East & Africa 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 45. Global 3D-Stacked Logic Chip Sales Quantity Market Share by Stacking Object (2021-2032)

Figure 46. Global 3D-Stacked Logic Chip Consumption Value Market Share by Stacking Object (2021-2032)

Figure 47. Global 3D-Stacked Logic Chip Average Price by Stacking Object (2021-2032) & (US\$/Unit)

Figure 48. Global 3D-Stacked Logic Chip Sales Quantity Market Share by Application (2021-2032)

Figure 49. Global 3D-Stacked Logic Chip Revenue Market Share by Application (2021-2032)

Figure 50. Global 3D-Stacked Logic Chip Average Price by Application (2021-2032) &

(US\$/Unit)

Figure 51. North America 3D-Stacked Logic Chip Sales Quantity Market Share by Stacking Object (2021-2032)

Figure 52. North America 3D-Stacked Logic Chip Sales Quantity Market Share by Application (2021-2032)

Figure 53. North America 3D-Stacked Logic Chip Sales Quantity Market Share by Country (2021-2032)

Figure 54. North America 3D-Stacked Logic Chip Consumption Value Market Share by Country (2021-2032)

Figure 55. United States 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 56. Canada 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 57. Mexico 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 58. Europe 3D-Stacked Logic Chip Sales Quantity Market Share by Stacking Object (2021-2032)

Figure 59. Europe 3D-Stacked Logic Chip Sales Quantity Market Share by Application (2021-2032)

Figure 60. Europe 3D-Stacked Logic Chip Sales Quantity Market Share by Country (2021-2032)

Figure 61. Europe 3D-Stacked Logic Chip Consumption Value Market Share by Country (2021-2032)

Figure 62. Germany 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 63. France 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 64. United Kingdom 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 65. Russia 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 66. Italy 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 67. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity Market Share by Stacking Object (2021-2032)

Figure 68. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity Market Share by Application (2021-2032)

Figure 69. Asia-Pacific 3D-Stacked Logic Chip Sales Quantity Market Share by Region (2021-2032)

Figure 70. Asia-Pacific 3D-Stacked Logic Chip Consumption Value Market Share by

Region (2021-2032)

Figure 71. China 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 72. Japan 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 73. South Korea 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 74. India 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 75. Southeast Asia 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 76. Australia 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 77. South America 3D-Stacked Logic Chip Sales Quantity Market Share by Stacking Object (2021-2032)

Figure 78. South America 3D-Stacked Logic Chip Sales Quantity Market Share by Application (2021-2032)

Figure 79. South America 3D-Stacked Logic Chip Sales Quantity Market Share by Country (2021-2032)

Figure 80. South America 3D-Stacked Logic Chip Consumption Value Market Share by Country (2021-2032)

Figure 81. Brazil 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 82. Argentina 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 83. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity Market Share by Stacking Object (2021-2032)

Figure 84. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity Market Share by Application (2021-2032)

Figure 85. Middle East & Africa 3D-Stacked Logic Chip Sales Quantity Market Share by Country (2021-2032)

Figure 86. Middle East & Africa 3D-Stacked Logic Chip Consumption Value Market Share by Country (2021-2032)

Figure 87. Turkey 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 88. Egypt 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 89. Saudi Arabia 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 90. South Africa 3D-Stacked Logic Chip Consumption Value (2021-2032) & (USD Million)

Figure 91. 3D-Stacked Logic Chip Market Drivers

Figure 92. 3D-Stacked Logic Chip Market Restraints

Figure 93. 3D-Stacked Logic Chip Market Trends

Figure 94. Porters Five Forces Analysis

Figure 95. Manufacturing Cost Structure Analysis of 3D-Stacked Logic Chip in 2025

Figure 96. Manufacturing Process Analysis of 3D-Stacked Logic Chip

Figure 97. 3D-Stacked Logic Chip Industrial Chain

Figure 98. Sales Channel: Direct to End-User vs Distributors

Figure 99. Direct Channel Pros & Cons

Figure 100. Indirect Channel Pros & Cons

Figure 101. Methodology

Figure 102. Research Process and Data Source

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