

The Global Photonics Packaging Market 2026-2036

<https://marketpublishers.com/r/G0A4E78A6675EN.html>

Date: March 2026

Pages: 0

Price: US\$ 1,500.00 (Single User License)

ID: G0A4E78A6675EN

Abstracts

Photonics packaging has entered a period of structural transformation with few parallels in the recent history of the semiconductor industry. What was once a specialised, largely bespoke activity confined to the manufacturing back end of optical transceiver production has become a strategic industrial priority — one that sits at the intersection of artificial intelligence infrastructure, advanced semiconductor packaging, next-generation display technology, and quantum computing hardware. This evolution is not incremental. It represents a fundamental redefinition of what photonics packaging is, what it is worth, and who in the supply chain captures that value.

For most of its commercial history, photonics packaging was anchored in optical transceivers for datacentre and telecommunications networks. The supply chain that emerged to serve this market was concentrated, efficient, and oriented around throughput and cost reduction. Companies such as Fabrinet, Jabil, and Luxshare dominated module assembly; foundries like TSMC and GlobalFoundries supplied the photonic integrated circuits; laser houses such as Coherent and Lumentum provided the III-V light sources. The result was a mature, well-optimised ecosystem well-suited to the requirements of pluggable transceiver manufacturing — but one whose architecture is now being disrupted at every level simultaneously.

The primary disruptive force is the explosive growth of generative artificial intelligence. Training and running large language models at the scale demanded by leading technology companies requires computing clusters of tens to hundreds of thousands of accelerators operating in tightly coupled parallel. The aggregate bandwidth these clusters require is extraordinary, and it cannot be delivered by conventional pluggable optical transceiver architectures within acceptable power budgets. The electrical path between a switch ASIC and a front-panel transceiver cage — involving PCB traces, connectors, and SerDes circuitry — consumes a growing and increasingly untenable fraction of total system power as signal speeds increase. Co-Packaged Optics solves

this by collapsing that electrical path from centimetres to millimetres, placing the optical engine directly on the same package substrate as the switch or compute chip. The result is a dramatic reduction in power per bit and a corresponding increase in achievable bandwidth density. This transition is not a future aspiration — first commercial CPO switch deployments occurred in 2026, and GPU-level optical interconnects are following closely behind.

The second major growth vector is augmented reality. The commercialisation of MicroLED display technology — combining gallium nitride light-emitting arrays at microscale pixel pitches with CMOS backplane integration — is creating a new and entirely distinct photonics packaging market. Achieving the brightness, resolution, and power efficiency required for mainstream consumer AR glasses demands mass transfer of millions of individual MicroLED dies onto CMOS backplanes at unprecedented precision and yield. This is a packaging challenge of a different character from datacom — characterised by display physics and consumer electronics form factors rather than network bandwidth — but one that requires equally demanding photonic integration expertise.

Beyond these two dominant growth engines, photonics packaging is expanding across FMCW LiDAR for automotive sensing, quantum computing hardware platforms, medical imaging, and defence sensing. Each application brings its own demanding packaging requirements: coherent detection stability across automotive temperature ranges for LiDAR; sub-0.01 dB coupling loss per interface for quantum photonics; radiation-hardened hermetic packages for aerospace. Together, these applications are converting photonics packaging from a single-segment market into a diversified, multi-application industry with structural growth characteristics.

Underpinning all of these trends is a technological transition of comparable importance to the shift from through-hole to surface-mount assembly in conventional electronics: the move from module-level assembly toward wafer-level heterogeneous integration. Foundries, advanced OSATs, and photonics design companies are converging on platforms — 2.5D silicon and glass interposers, fan-out wafer-level packaging, hybrid bonding — that enable photonic and electronic chiplets to be co-integrated at the wafer scale using lithographically defined alignment rather than active mechanical servo control. This transition raises the packaging content value per unit, compresses alignment tolerances, and moves the locus of competitive advantage upstream from module assembly houses toward foundries and design-driven packaging platforms.

Standardisation is the critical variable that will determine how quickly these transitions

reach production scale. Process Design Kits, Assembly Design Kits, CPO fibre interface standards, and common electrical interface specifications between switch ASICs and optical engines are all in active development — but none is yet mature. The pace at which industry consortia including the Optical Networking Forum, the Co-Packaged Optics Alliance, and SEMI can establish and promote these standards will materially influence the trajectory of the market across the forecast decade.

The Global Photonics Packaging Market 2026–2036 is the first dedicated market research report to define, quantify, and forecast photonics packaging as a standalone global market across a ten-year horizon. The report is based on primary interviews with over 80 industry stakeholders — including foundries, advanced OSATs, PIC designers, module assemblers, equipment vendors, hyperscalers, and quantum hardware developers — combined with a bottom-up modelling approach that builds market size estimates from unit volumes, packaging content values, and technology mix assumptions at the individual application and product level.

The report defines photonics packaging as the complete set of materials, processes, equipment, and intellectual property involved in assembling photonic integrated circuits and optical components into functional modules and systems. This encompasses module-level assembly, hybrid and heterogeneous integration of photonic and electronic dies, wafer-level packaging, fiber-to-chip coupling, and precision alignment processes. It explicitly excludes the intrinsic fabrication cost of photonic or electronic chips themselves, focusing on the packaging value added across the supply chain.

Six application segments are covered in full: optical transceivers for datacom and telecom; co-packaged optics for AI datacentre switches and GPU interconnects; augmented reality display engines; automotive FMCW LiDAR; quantum computing and quantum networking; and other applications including medical imaging, defence, and industrial sensing. Each segment receives dedicated technology analysis, supply chain mapping, competitive landscape assessment, and a quantitative ten-year forecast with annual granularity from 2026 to 2036.

The technology coverage spans the complete spectrum of photonics packaging approaches currently in production or development — from conventional wire bond and flip-chip module assembly through fan-out wafer-level packaging, 2.5D silicon and glass interposer integration, 3D micro-bump stacking, Cu-Cu hybrid bonding, and ultimately monolithic photonic-electronic integration. The report provides comparative benchmarks of all major platforms, traces the evolution of fiber-to-chip coupling from V-groove arrays to photonic wire bonding and detachable CPO connectors, and maps the progression of

EIC/PIC integration from 2D through to SoIC hybrid bonding. Technology roadmaps are provided for the full forecast period.

Co-Packaged Optics receives a dedicated chapter of particular depth, covering the definition and architecture of optical engines, a detailed comparison with pluggable optics, the AI datacentre network hierarchy and switch ASIC bandwidth scaling trajectory, the divergent CPO ecosystem strategies of NVIDIA and Broadcom, the three CPO packaging structure types, and a comprehensive suite of quantitative forecasts covering GPU optical I/O units and revenue, CPO network switch units and revenue, total CPO market overview, technology mix by integration architecture, and a generation-by-generation scale-out network system roadmap through 2036.

The ecosystem and supply chain analysis maps ten value chain segments from raw wafer to end-customer system deployment, with revenue and margin profiles for each. Regional analysis covers Taiwan, North America, Europe, and Asia-Pacific. The competitive landscape chapter addresses market share by player and segment, M&A and partnership activity from 2023 to 2026, vertical integration trends, and a strategic outlook through 2036. The report includes 71 data tables, 35 figures, and detailed profiles of 69 companies across the full photonics packaging value chain.

Report Contents include

Chapter 1: Executive Summary — key findings, market definition and scope, drivers and restraints, market size and growth, strategic implications by stakeholder type

Chapter 2: Market Context and Background — historical evolution, AI-driven growth catalysts, semiconductor packaging overview, photonics packaging vs conventional semiconductor packaging, standardisation imperative

Chapter 3: Technology Landscape — light source integration approaches, wafer-level packaging, 2.5D and 3D packaging, hybrid bonding, interconnection techniques, fiber-to-chip coupling, EIC/PIC integration, module-level packaging, solutions for quantum, technology roadmap 2026–2036

Chapter 4: Co-Packaged Optics — CPO definition and architecture, optical engine composition, CPO vs pluggable comparison, AI datacenter architecture, NVIDIA vs Broadcom strategies, CPO packaging structures, full market forecasts 2026–2036, challenges matrix

Chapter 5: Application Segments — optical transceivers, AI datacentres, augmented reality, automotive FMCW LiDAR, quantum technologies, medical/defence/industrial

Chapter 6: Ecosystem and Supply Chain — value chain overview and margin profiles, supply chain analysis by segment, regional ecosystem analysis (Taiwan, North America, Europe, Asia-Pacific)

Chapter 7: Global Market Forecasts 2026–2036 — total market, segment forecasts, technology mix forecasts, regional forecasts

Chapter 8: Competitive Landscape — market share analysis, M&A activity, vertical integration trends, competitive dynamics 2026–2036

Chapter 9: Company Profiles — 79 profiles covering the full value chain

The report profiles 79 companies spanning the complete photonics packaging ecosystem including Aeva, Amkor Technology, Anello Photonics, Ansys, Applied Materials, ASE Group, ASM AMICRA, ASMPT, Aurora Innovation, AyarLabs, Bay Photonics, Broadcom, Cisco, Corning Incorporated, Diamond Photonics, Eoptolink, EV Group, Fabrinet, FEMTOprint, Ficontec, Finetech, FOXCONN, GIS, Goertek, Google, ICON Photonics, IMEC, Innolight, IonQ, izmo Microsystems, Jabil, JBD (Jade Bird Display), LAM Research, Lightmatter and more...

Contents

1 EXECUTIVE SUMMARY

- 1.1 Report Overview and Key Findings
- 1.2 Market Definition and Scope
 - 1.2.1 Definition of Photonics Packaging
 - 1.2.2 Boundary Between Photonics Packaging and Broader Semiconductor Packaging
 - 1.2.3 Scope: Applications Addressed in This Report
- 1.3 Key Market Drivers and Restraints
- 1.4 Market Size and Growth
- 1.5 Photonics Packaging: From Backend Activity to Strategic Enabler
- 1.6 Photonics Packaging in the AI Era
- 1.7 The Shift to Advanced Packaging: From Module-Level to Wafer-Level Integration
- 1.8 Competitive and Ecosystem Snapshot
- 1.9 Key Conclusions and Strategic Implications

2 MARKET CONTEXT AND BACKGROUND

- 2.1 Photonics Packaging: Historical Evolution
 - 2.1.1 Origins in Optical Transceivers for Datacom and Telecom
 - 2.1.2 The Shift Toward Heterogeneous Integration
 - 2.1.3 AI-Driven Bandwidth Demand as a Structural Growth Catalyst
- 2.2 Photonics in the AI Era
 - 2.2.1 The Explosive Growth of Generative AI and LLMs
 - 2.2.2 Compute Demand Scaling and Network Bottlenecks
 - 2.2.3 The Role of Optical Interconnects in AI Infrastructure
- 2.3 Semiconductor Packaging Technology Overview
 - 2.3.1 Conventional Packaging Approaches
 - 2.3.2 Advanced Packaging Approaches
 - 2.3.3 From 1D to 3D Integration: The Packaging Evolution Continuum
- 2.4 Why Photonics Packaging Differs from Conventional Semiconductor Packaging
- 2.5 The Standardization Imperative
 - 2.5.1 PDK and ADK-Driven Design Environments
 - 2.5.2 Role of Standards Bodies and Industry Consortia
 - 2.5.3 Barriers to High-Volume Photonics Packaging Deployment

3 TECHNOLOGY LANDSCAPE

- 3.1 Light Source Integration Technologies
 - 3.1.1 Integration Approach Overview
 - 3.1.2 Hybrid Integration
 - 3.1.3 Heterogeneous Integration
 - 3.1.4 Heterogeneously Integrated Light Sources on Silicon Photonics (for Pluggables)
 - 3.1.5 MicroLED-on-Si Hybridization
- 3.2 Advanced Packaging Technologies for Photonics
 - 3.2.1 Wafer-Level Packaging (WLP)
 - 3.2.1.1 Wafer-Level Chip Scale Packaging (WLCSP)
 - 3.2.1.2 Fan-Out Wafer-Level Packaging (FO-WLP)
 - 3.2.1.3 WLP Manufacturing Processes
 - 3.2.2 2.5D and 3D Packaging
 - 3.2.2.1 Silicon Interposer 2.5D (Through-Silicon Via)
 - 3.2.2.2 Organic-Based 2.5D Packaging
 - 3.2.2.3 Glass-Based 2.5D Packaging
 - 3.2.2.4 3D Stacked Packages
 - 3.2.3 Hybrid Bonding
 - 3.2.3.1 Fusion Bond and Direct Molecular Bonding
 - 3.2.3.2 Cu-Cu Bumpless Hybrid Bonding
 - 3.2.3.3 Devices Using Hybrid Bonding
 - 3.2.4 Photonics-Compatible Advanced Packaging Platform Comparison
- 3.3 Interconnection Techniques in Photonics Packaging
 - 3.3.1 Wire Bonding
 - 3.3.2 Flip-Chip Bumping
 - 3.3.3 Micro-Bumping
 - 3.3.4 Through-Silicon Via (TSV)
 - 3.3.5 Redistribution Layer (RDL)
 - 3.3.6 Photonic Wire Bonding
- 3.4 Fiber-to-Chip Coupling
 - 3.4.1 Fiber-to-Chip Coupling Modalities Overview
 - 3.4.2 V-Groove Technology: From 260µm to 130µm Pitch
 - 3.4.3 Detachable Fiber-to-Chip Couplers
 - 3.4.4 Serviceability and Detachability Design Considerations
 - 3.4.5 Fiber Array Units (FAUs) and Connectorization
- 3.5 EIC/PIC Integration
 - 3.5.1 Photonic Integrated Circuits (PICs) — Key Concepts
 - 3.5.1.1 What are PICs? Material Platforms and Integration Levels
 - 3.5.1.2 PICs vs Silicon Photonics — Differences and Overlap
 - 3.5.2 Electronic-Photonic Integration Requirements

- 3.5.3 2D EIC/PIC Integration
- 3.5.4 2.5D EIC/PIC Integration
- 3.5.5 3D EIC/PIC Integration
- 3.5.6 3D Optical Engine Configuration Examples
 - 3.5.6.1 Configuration 1: EIC-on-PIC with Micro-Bumps
 - 3.5.6.2 Configuration 2: PIC-on-EIC with Through-Silicon Vias
 - 3.5.6.3 Configuration 3: 3D SoIC with Hybrid Bonding
- 3.5.7 TSMC's Role in Heterogeneous EIC/PIC Integration
- 3.6 Module-Level Packaging
 - 3.6.1 Optical Transceiver Module Architecture
 - 3.6.2 Typical Process Steps and Major Equipment Suppliers
 - 3.6.3 Which Packaging Approach for Which Application?
 - 3.6.4 Solutions for Quantum Packaging
- 3.7 Technology Roadmap
 - 3.7.1 Long-Term Technology Evolution Roadmap 2026–2036
 - 3.7.2 Long-Term Evolution of Co-Packaged Optics

4 CO-PACKAGED OPTICS (CPO)

- 4.1 Introduction to Co-Packaged Optics
 - 4.1.1 Definition and Core Concepts
 - 4.1.1.1 Concept 1: Proximity Integration
 - 4.1.1.2 Concept 2: Functional Partitioning
 - 4.1.1.3 Concept 3: Coherent Ecosystem Development
 - 4.1.2 What is an Optical Engine (OE)?
 - 4.1.2.1 Optical Engine Composition and Components
 - 4.1.2.2 Optical Engine vs Pluggable Transceiver
 - 4.1.2.3 Critical Performance Parameters
 - 4.1.3 Key Technology Building Blocks for CPO
 - 4.1.3.1 Silicon Photonics PIC
 - 4.1.3.2 Electronic IC (EIC)
 - 4.1.3.3 External Laser Sources and Optical Power Supply
- 4.2 CPO vs Pluggable Optics
 - 4.2.1 Pluggable Optics — Current Status, Bottlenecks and Limitations
 - 4.2.1.1 Form Factor Constraints
 - 4.2.1.2 Electrical Interface and SerDes Limitations
 - 4.2.1.3 Thermal Management Challenges
 - 4.2.1.4 On-Board Optics (OBO) as a Transitional Step
 - 4.2.2 Power Efficiency Comparison: CPO vs Pluggable vs Copper

- 4.2.3 Design Decisions: Choosing Between CPO and Pluggables
- 4.3 Data Centre Architecture and CPO Applications
 - 4.3.1 Modern High-Performance AI Data Centre Architecture
 - 4.3.1.1 Physical Infrastructure Hierarchy
 - 4.3.1.2 Network Architecture: Scale-Out and Scale-Up
 - 4.3.1.3 Power and Cooling Considerations
 - 4.3.2 Switches: Key Components in AI Data Centres
 - 4.3.2.1 Switch Architecture Evolution
 - 4.3.2.2 Switch ASIC Technology and Bandwidth Scaling
 - 4.3.3 Scale-Out Network Switching Applications
 - 4.3.4 Scale-Up Computing Optical I/O Applications
 - 4.3.5 NVIDIA vs Broadcom: Strategic Comparison in AI Infrastructure and CPO
 - 4.3.5.1 NVIDIA's CPO Strategy: Vertical Integration
 - 4.3.5.2 Broadcom's CPO Strategy: Open Ecosystem
 - 4.3.5.3 Competitive Dynamics
 - 4.3.6 L2 Frontside Network Architecture: CPO vs Non-CPO
 - 4.3.7 Migration from Copper to Optical Interconnects in AI Systems
- 4.4 CPO Packaging Structures
 - 4.4.1 Types of CPO + XPU/Switch ASIC Packaging Structures
 - 4.4.1.1 Type I: Optical Engines on Package Periphery
 - 4.4.1.2 Type II: Optical Engines Co-Located with ASIC on Interposer
 - 4.4.1.3 Type III: 3D Stacked Optical Engines
 - 4.4.2 System Integration of Network Switches by Packaging Technologies
 - 4.4.3 System Integration of Optical I/O by Packaging Technologies
- 4.5 CPO Market Forecasts 2026–2036
 - 4.5.1 Server Boards, CPUs and GPUs/Accelerators Shipment Forecast
 - 4.5.2 Optical I/O for AI Interconnect CPO Forecast (Units Shipped)
 - 4.5.3 Optical I/O for AI Interconnect CPO Forecast (Revenue)
 - 4.5.4 CPO Network Switches for AI Accelerators (Units Shipped)
 - 4.5.5 CPO Network Switches for AI Accelerators (Market Size)
 - 4.5.6 Total CPO Market Overview
 - 4.5.7 CPO by EIC/PIC Integration Technology (Unit Shipments)
 - 4.5.8 CPO Roadmap: Scale-Out Networks
- 4.6 CPO Challenges and Future Potential
 - 4.6.1 Technical Challenges
 - 4.6.2 Commercial and Standardization Challenges
 - 4.6.3 Future Potential and Outlook

5 APPLICATION SEGMENTS

5.1 Telecom and Datacom

5.1.1 Optical Transceiver Market Overview

5.1.2 Photonics Packaging for Optical Transceivers

5.1.3 Market Forecast: Optical Transceivers 2026–2036

5.1.4 Transition from Pluggable to Co-Packaged: Hybrid Period 2026–2030

5.1.5 Supply Chain Concentration and Verticality Trends

5.2 AI Data Centres

5.2.1 AI Data Centre Photonics Packaging Demand

5.2.2 Hyperscaler Capex and Photonics Intensity

5.2.3 Current AI System Architecture: NVIDIA DGX/HGX Platforms

5.2.4 Future AI Architecture (Short to Mid-Term: 2026–2030)

5.2.5 Future AI Architecture (Long-Term: 2031–2036)

5.3 Augmented Reality Displays

5.3.1 Consumer AR Market Overview and Inflection Point (2026–2028)

5.3.2 Display Engine Technologies for AR

5.3.2.1 LCoS-Based Optical Engines

5.3.2.2 MicroLED-Based Optical Engines

5.3.2.3 Laser-Based Architectures and New Coupling Challenges

5.3.2.4 LCoS to MicroLED 2026–2036

5.3.3 AR Photonics Packaging: Form Factor as Key Differentiator

5.3.4 Market Forecast: AR Display Volumes 2026–2036

5.3.5 Market Forecast: AR Packaging Revenue 2026–2036

5.3.6 Microdisplay Supply Chain: MicroLED Focus

5.4 Automotive: FMCW LiDAR

5.4.1 FMCW LiDAR Technology and Photonics Packaging Requirements

5.4.2 FMCW LiDAR Photonics Integration Challenges

5.4.3 Market Forecast: FMCW LiDAR Volume and Packaging Revenue 2026–2036

5.5 Quantum Technologies

5.5.1 Photonics as the Hidden Bottleneck in Scalable Quantum Technologies

5.5.2 Photonics in Quantum Computer Architectures

5.5.2.1 Photonic Quantum Computers

5.5.2.2 Trapped-Ion Quantum Systems

5.5.2.3 Neutral Atom Quantum Systems

5.5.3 Photonics Packaging Requirements for Quantum

5.5.3.1 Ultra-Low-Loss Fiber Alignment

5.5.3.2 High-Density Laser Integration for Qubit Scaling

5.5.3.3 Extreme Precision Assembly

5.5.4 Quantum Photonics Packaging Solutions and Outlook

5.6 Other Application Segments

6 ECOSYSTEM AND SUPPLY CHAIN

6.1 Photonics Packaging Value Chain Overview

6.1.1 Generic Value Chain: From Die to System

6.1.2 Value Capture by Chain Segment

6.2 Supply Chain Analysis by Segment

6.2.1 PIC Design Segment

6.2.2 ASIC and xPU Design Segment

6.2.3 Laser Sources Segment

6.2.4 SOI Wafer and Epi-Wafer Segment

6.2.5 EIC, Retimers, SerDes and PHY Segment

6.2.6 Connectors and Fibers Segment

6.2.7 Foundries Segment

6.2.8 Packaging, Assembling and Testing Segment

6.2.9 System and Equipment Segment

6.2.10 End Customers (Hyperscalers) Segment

6.2.11 Ecosystem Interdependencies and Strategic Implications

6.3 Regional Ecosystem Analysis

6.3.1 The Taiwanese Ecosystem

6.3.2 NVIDIA's Ecosystem

6.3.3 The European Ecosystem

6.3.4 North American Ecosystem

6.3.5 Asia-Pacific (Excluding Taiwan) Ecosystem

7 GLOBAL MARKET FORECASTS 2026–2036

7.1 Overall Market Forecast

7.1.1 Total Global Photonics Packaging Market: Revenue (\$M) 2026–2036

7.1.2 Market Revenue by Application Segment

7.1.3 Market Revenue by Packaging Technology

7.2 Segment Forecasts

7.2.1 Optical Transceivers (Datacom & Telecom)

7.2.2 Co-Packaged Optics (CPO)

7.2.3 Augmented Reality

7.2.4 Automotive LiDAR (FMCW)

7.2.5 Quantum Technologies

7.2.6 Other Applications (Medical, Defense, Industrial)

7.3 Regional Forecasts

7.3.1 Regional Analysis

8 COMPETITIVE LANDSCAPE

8.1 Competitive Environment Overview

8.2 2 Market Share Analysis

8.3 Positioning and M&A Activity

8.4 Vertical Integration Trends

8.5 Future Outlook: Competitive Dynamics 2026–2036

9 COMPANY PROFILES (79 COMPANY PROFILES)

10 APPENDIX

10.1 Definitions & Terminology

10.2 Research Methodology

11 REFERENCES

List Of Tables

LIST OF TABLES

- Table 1. Photonics Packaging Market at a Glance — Revenue (\$M) 2026–2036
- Table 2. Key Market Metrics and CAGR Summary by Segment
- Table 3. Application Segments and Packaging Value Chain Boundaries
- Table 4. Market Drivers, Restraints, Opportunities and Threats (DROT Framework)
- Table 5. Global Photonics Packaging Market Revenue (\$M), 2026–2036
- Table 6. Market Revenue by Application Segment (%), 2026-2036
- Table 7. Key Milestones in Photonics Packaging Technology Development
- Table 8. Semiconductor Packaging Technology Landscape — Conventional to Advanced
- Table 9. Conventional vs Advanced Packaging — Feature and Performance Comparison
- Table 10. Key Differences Between Electronic and Photonic Packaging Requirements
- Table 11. Integration Approach Comparison at a Glance
- Table 12. WLP Variants — Characteristics, Benefits and Photonics Applications
- Table 13. 2.5D vs 3D Packaging — Performance, Cost and Complexity Trade-offs
- Table 14. Fan-Out vs Hybrid Bonding — Photonics-Compatible Platform Comparison
- Table 15. Photonics-Compatible Advanced Packaging Platform Benchmark
- Table 16. Interconnection Technique Comparison — Electrical and Optical Performance
- Table 17. Fiber-to-Chip Coupling Modalities Comparison
- Table 18. Fiber-to-Chip Coupling Methods — Edge Coupling vs Grating Coupling vs Lensed Fiber
- Table 19. Coupling Technology Supplier Landscape
- Table 20. Benchmark of Packaging Technologies for EIC/PIC Integration
- Table 21. Typical Process Steps and Key Equipment Suppliers for Photonics Packaging
- Table 22. Integrated Optics for Datacom — Process and Integration Roadmap
- Table 23. Packaging Technology Selection Matrix by Application Segment
- Table 24. CPO Key Technology Building Blocks — Specifications and Suppliers
- Table 25. Transmission Losses in Pluggable vs CPO Connections
- Table 26. Pluggable Optics vs CPO — Performance, Cost and Operational Comparison
- Table 27. Power Consumption Breakdown — CPO vs Pluggable Optics vs Copper Interconnects
- Table 28. Decision Framework — CPO vs Pluggables by Use Case
- Table 29. Scale-Up vs Scale-Out — Volume Forecast 2026–2036 (Units)
- Table 30. CPO Product Benchmark — NVIDIA vs Broadcom
- Table 31. NVIDIA and Broadcom — Divergent CPO Ecosystem Strategies
- Table 32. Supporting data — Copper vs Optical Benchmark by Parameter
- Table 33. Copper vs Optical — Benchmark for High-Bandwidth AI Systems
- Table 34. CPO Packaging Structure Benchmark by Integration Type

- Table 35. System Integration of Optical I/O by Packaging Technology 2026–2036
- Table 36. Server Board, CPU and GPU/Accelerator Shipment Forecast 2026–2036
- Table 37. Optical I/O for AI Interconnect CPO — Units Shipped 2026–2036
- Table 38. Optical I/O for AI Interconnect CPO — Revenue (\$M) 2026–2036
- Table 39. CPO Network Switches — Units Shipped Forecast 2026–2036
- Table 40. CPO Network Switches — Revenue (\$M) Forecast 2026–2036
- Table 41. Total CPO Market Revenue (\$M) and Units — 2026–2036 Overview
- Table 42. Total CPO by EIC/PIC Integration Technology — Unit Shipments 2026–2036
- Table 43. CPO Challenges — Technical and Commercial Assessment Matrix
- Table 44. Optical Transceiver Market Segmentation
- Table 45. Photonics Packaging for Optical Transceivers — Revenue Forecast (\$M) 2026–2036
- Table 46. Optical Transceiver Packaging Market Share by Key Players 2026
- Table 47. AI Data Centre Photonics Packaging Demand by Segment 2026–2036 (\$M)
- Table 48. Display Engine Technology Comparison for AR Applications
- Table 49. AR Market Forecast — Volume (Units) 2026–2036
- Table 50. Display Engines for AR — Volume Forecast 2026–2036
- Table 51. AR Display Engine Packaging Revenue Forecast (\$M) by Technology 2026–2036
- Table 52. FMCW LiDAR Photonics Packaging Revenue Forecast (\$M) 2026–2036
- Table 53. Key Players in FMCW LiDAR Photonics Packaging
- Table 54. Map of Quantum Companies— By Photonics-Based Approach
- Table 55. Quantum Technology Photonics Packaging Requirements by Platform
- Table 56. Quantum Photonics Packaging Solutions Landscape
- Table 57. Other Application Segments — Market Characteristics and Packaging Requirements
- Table 58. Value Chain Segment — Revenue and Margin Profile
- Table 59. Supply Chain Segments — Key Players by Tier
- Table 60. Global Photonics Packaging Market Revenue (\$M) 2026–2036 by Segment
- Table 61. Photonics Packaging Market Revenue Share by Segment (%), 2026 vs 2036
- Table 62. Photonics Packaging Market Revenue by Technology (\$M) 2026–2036
- Table 63. OT Packaging Revenue by Sub-Segment (\$M)
- Table 64. CPO Revenue by Sub-Segment (\$M)
- Table 65. AR Packaging Revenue by Technology (\$M)
- Table 66. FMCW LiDAR Packaging Revenue by Application (\$M)
- Table 67. Quantum Photonics Packaging Revenue by Platform (\$M)
- Table 68. Other Applications Packaging Revenue (\$M)
- Table 69. Regional Photonics Packaging Market Forecast (\$M) 2026–2036
- Table 70. Market Share by Key Player and Segment 2026

Table 71. Notable M&A and Partnership Activity in Photonics Packaging 2023–2026

Table 72. Strategic Outlook — Key Competitive Moves by Player Tier 2026–2036

Table 73. Glossary of Key Terms and Abbreviations

Table 74. Report Scope — Applications, Technologies and Geographies Covered

List Of Figures

LIST OF FIGURES

- Figure 1. Photonics Packaging Market at a Glance — Revenue (\$M) 2026–2036
- Figure 2. Market Revenue by Application Segment (%), 2026-2036
- Figure 3. AI Datacenter Network Hierarchy — Scale-Out and Scale-Up Networks
- Figure 4. Evolution from Hybrid to Heterogeneous Integration in Photonics Packaging
- Figure 5. Photonics Packaging Ecosystem Map — Key Players by Value Chain Segment
- Figure 6. Historical Evolution of Photonics Packaging Architectures
- Figure 7. Generative AI Compute Demand Scaling vs. Electrical Interconnect Capacity
- Figure 8. Photonics Packaging Standardization Roadmap
- Figure 9. Integration Approach Spectrum — Hybrid to Monolithic
- Figure 10. Heterogeneous Light Source Integration on Silicon Photonics
- Figure 11. Wafer-Level Packaging Process Flow
- Figure 12. 2.5D vs 3D Packaging Architecture Comparison
- Figure 13. Hybrid Bonding Architecture and Process
- Figure 14. V-Groove Pitch Evolution Roadmap
- Figure 15. Detachable Fiber-to-Chip Coupler Architecture
- Figure 16. PIC Architecture — Transmit and Receive Path
- Figure 17. 3D Optical Engine Configuration Examples
- Figure 18. Optical Transceiver at the Module Level — 400G Architecture
- Figure 19. Photonics Packaging Technology Trends Roadmap 2026–2036
- Figure 20. Long-Term CPO Integration Architecture Evolution
- Figure 21. Optical Engine Architecture and Transmit/Receive Path
- Figure 22. CPO vs Non-CPO Network Architecture Diagram
- Figure 23. Copper-to-Optical Migration Roadmap for High-End AI Systems
- Figure 24. System Integration of Network Switches by Packaging Technology 2026–2036
- Figure 25. CPO System Roadmap for Scale-Out Networks
- Figure 26. Optical Transceiver at the Module Level — Key Components
- Figure 27. Optical Transceiver Packaging — Module-Level Anatomy
- Figure 28. Technology Migration Path — Pluggables to CPO Timeline
- Figure 29. Current and Future AI System Architecture Comparison
- Figure 30. Consumer AR Technology Roadmap — LCoS to MicroLED 2026–2036
- Figure 31. Microdisplay Supply Chain Map — MicroLED Focus
- Figure 32. Progression of FMCW LiDAR — Technology Architecture
- Figure 33. Photonics in Quantum Computer Architectures — By Technology Platform
- Figure 34. Photonics Packaging Value Chain Overview
- Figure 35. Generic Outline of Optical Modules in the Data Centre Value Chain

Figure 36. CPO Industrial Ecosystem — Full Supply Chain Map

Figure 37. Taiwanese Photonics Packaging Ecosystem

Figure 38. NVIDIA's Photonics Packaging Ecosystem

Figure 39. Aeries II LiDAR system.

Figure 40. NVIDIA's silicon photonics switches.

I would like to order

Product name: The Global Photonics Packaging Market 2026-2036

Product link: <https://marketpublishers.com/r/G0A4E78A6675EN.html>

Price: US\$ 1,500.00 (Single User License / Electronic Delivery)

If you want to order Corporate License or Hard Copy, please, contact our Customer Service:

info@marketpublishers.com

Payment

To pay by Credit Card (Visa, MasterCard, American Express, PayPal), please, click button on product page <https://marketpublishers.com/r/G0A4E78A6675EN.html>