

The Global Market for Advanced Semiconductor Packaging 2024-2035

<https://marketpublishers.com/r/GD603A622464EN.html>

Date: March 2024

Pages: 330

Price: US\$ 1,550.00 (Single User License)

ID: GD603A622464EN

Abstracts

The global landscape of semiconductor manufacturing is rapidly evolving, with advanced packaging emerging as a critical component of manufacturing and design. It affects power, performance, and cost on a macro level, and the basic functionality of all chips on a micro level. Advanced packaging allows for the creation of faster, cost-effective systems by integrating various chips, a technique that's increasingly essential given the physical limitations of traditional chip miniaturization. It is reshaping the industry, enabling the integration of diverse chip types and enhancing processing speeds.

The U.S. government recognizes the importance of advanced packaging and has introduced a \$3 billion National Advanced Packaging Manufacturing Program aimed at establishing high-volume packaging facilities by the end of the decade. The focus on packaging complements the existing efforts under the CHIPS and Science Act, emphasizing the interconnectedness of chipmaking and packaging.

The Global Market for Advanced Semiconductor Packaging 2024-2035 provides a comprehensive analysis of the global advanced semiconductor packaging technologies market from 2020-2035. It encompasses packaging approaches like wafer-level packaging, 2.5D/3D integration, chiplets, fan-out, and flip chip, analyzing market values in the billions (USD) by type, region, and end-use application.

Trends analyzed include heterogeneous integration, interconnects, thermal solutions, miniaturization, supply chain maturity, simulation/data analytics. Leading companies profiled include TSMC, Samsung, Intel, JCET, Amkor. Applications covered include AI, mobile, automotive, aerospace, IoT, communications (5G/6G), high performance computing, medical, and consumer electronics.

Regional markets explored include North America, Asia Pacific, Europe, China, Japan, and RoW. The report also assesses drivers like ML/AI, data centers, EV/ADAS; challenges like costs, complexity, reliability; emerging approaches like system-in-package, monolithic 3D ICs, advanced substrates, novel materials. Overall an in-depth benchmark analysis of the opportunities within the advancing semiconductor packaging industry.

Report contents include:

Market size and forecasts

Key technology trends

Growth drivers and challenges

Competitive landscape analysis

Future packaging trends outlook

In-depth analysis of wafer level packaging (WLP)

System-in-Package (SiP) and heterogeneous integration

Monolithic 3D ICs overview

Advanced semiconductor packaging applications across key markets: AI, mobile, automotive, aerospace, IoT, communications, HPC, medical, consumer electronics

Regional market breakdown

Assessment of key industry challenges: complexity, costs, supply chain maturity, standards

Company profiles: Strategies and technologies of 90 key players. Companies profiled include 3DSEMI, Amkor, Chipbond, ChipMOS, Intel Corporation, Leader-Tech Semiconductor, Powertech, Samsung Electronics, Silicon Box, SJ Semiconductor Corp., SK hynix, SPIL, Tongfu, Taiwan Semiconductor

Manufacturing Company (TSMC) and Yuehai Integrated (Full list of companies profiled in table of contents).

Contents

1 RESEARCH METHODOLOGY

2 EXECUTIVE SUMMARY

2.1 Semiconductor Packaging Technology Overview

2.1.1 Key challenges

2.1.2 Evolution of semiconductor packaging

2.1.2.1 From 1D to 3D

2.1.3 Conventional packaging approaches

2.1.4 Advanced packaging approaches

2.2 Semiconductor Supply Chain

2.3 Advanced Packaging Supply Chain

2.4 Key Technology Trends in Advanced Packaging

2.5 Market Growth Drivers

2.6 Competitive Landscape

2.7 Market Challenges

2.8 Future outlook

2.8.1 Heterogeneous Integration

2.8.2 Chiplets and Die Disaggregation

2.8.3 Advanced Interconnects

2.8.4 Scaling and Miniaturization

2.8.5 Thermal Management

2.8.6 Materials Innovation

2.8.7 Supply Chain Developments

2.8.8 Role of Simulation and Data Analytics

3 SEMICONDUCTOR PACKAGING TECHNOLOGIES

3.1 Transistor Device Scaling

3.1.1 Overview

3.1.2 Heterogeneous Architecture Transition

3.1.3 Co-Design Focus Areas

3.2 Wafer Level Packaging

3.3 Fan-Out Wafer Level Packaging

3.4 Chiplets

3.4.1 AMD EPYC and Ryzen processor families

3.4.2 Disaggregation Needs

3.5 Interconnection in Semiconductor Packaging

3.5.1 Overview

3.5.2 Wire Bonding

3.5.3 Flip-chip bonding

3.5.4 Interposer

3.5.5 Through-silicon via (TSV) bonding

3.5.6 Hybrid bonding with chiplets

3.6 2.5D and 3D Packaging

3.6.1 2.5D packaging

3.6.1.1 Overview

3.6.1.1.1 Silicon Interposer 2.5D

3.6.1.1.1.1 Through Si Via (TSV)

3.6.1.1.1.2 (SiO₂) based redistribution layers (RDLs)

3.6.1.1.2 2.5D Organic-based packaging

3.6.1.1.2.1 Chip-first and chip-last fan-out packaging

3.6.1.1.2.2 Organic substrates

3.6.1.1.2.3 Organic RDL

3.6.1.1.3 2.5D glass-based packaging

3.6.1.1.3.1 Benefits

3.6.1.1.3.2 Glass Si interposers in advanced packaging

3.6.1.1.3.3 Glass material properties

3.6.1.1.3.4 2/2 μm line/space metal pitch on glass substrates

3.6.1.1.3.5 3D Glass Panel Embedding (GPE) packaging

3.6.1.1.3.6 Thermal management

3.6.1.1.3.7 Polymer dielectric films

3.6.1.1.3.8 Challenges

3.6.1.1.3.9 Comparison with other substrates

3.6.1.1.4 2.5D vs. 3D Packaging

3.6.1.2 Benefits

3.6.1.3 Challenges

3.6.1.4 Trends

3.6.1.5 Market players

3.6.2 3D packaging

3.6.2.1 Overview

3.6.2.1.1 Conventional 3D packaging

3.6.2.1.2 Advanced 3D Packaging with through-silicon vias (TSVs)

3.6.2.1.3 Three-dimensional (3D) hybrid bonding

3.6.2.1.3.1 Devices using hybrid bonding

3.6.2.2 3D Microbump technology

- 3.6.2.2.1 Technologies
- 3.6.2.2.2 Challenges
- 3.6.2.2.3 Bumpless copper-to-copper (Cu-Cu) hybrid bonding
- 3.6.2.3 Trends

4 WAFER-LEVEL PACKAGING

- 4.1 Introduction
- 4.2 Benefits
- 4.3 Types of Wafer Level Packaging
 - 4.3.1 Wafer Level Chip Scale Packaging
 - 4.3.1.1 Overview
 - 4.3.1.2 Advantages
 - 4.3.1.3 Applications
 - 4.3.2 Wafer Level Fan-Out Packaging
 - 4.3.2.1 Overview
 - 4.3.2.2 Advantages
 - 4.3.2.3 Applications
 - 4.3.3 Wafer Level Fan-In Packaging
 - 4.3.3.1 Overview
 - 4.3.3.2 Advantages
 - 4.3.3.3 Applications
 - 4.3.4 Other Types of WLP
 - 4.3.4.1 Cu-Pillar Flip Chip
 - 4.3.4.2 Advantages
 - 4.3.4.2.1 Applications
 - 4.3.4.3 Embedded Wafer Level BGA (eWLB)
 - 4.3.4.4 Advantages
 - 4.3.4.4.1 Applications
 - 4.3.4.5 Chip-last FO-WLP
 - 4.3.4.5.1 Advantages
 - 4.3.4.5.2 Applications
 - 4.3.4.6 Wafer-on-Wafer (WoW)
 - 4.3.4.6.1 Applications
- 4.4 WLP Manufacturing Processes
 - 4.4.1 Wafer Preparation
 - 4.4.2 RDL Buildup
 - 4.4.3 Bumping
 - 4.4.4 Encapsulation

- 4.4.5 Integration
- 4.4.6 Test and Singulation
- 4.5 Wafer Level Packaging Trends
- 4.6 Applications of Wafer Level Packaging
 - 4.6.1 Mobile and Consumer Electronics
 - 4.6.2 Automotive Electronics
 - 4.6.3 IoT and Industrial
 - 4.6.4 High Performance Computing
 - 4.6.5 Aerospace and Defense
- 4.7 Wafer Level Packaging Outlook

5 SYSTEM-IN-PACKAGE AND HETEROGENEOUS INTEGRATION

- 5.1 Introduction
- 5.2 Approaches for heterogenous integration
 - 5.2.1 Technology Building Blocks
- 5.3 SiP Manufacturing Approaches
 - 5.3.1 2.5D Integrated Interposers
 - 5.3.2 Multi-Chip Modules
 - 5.3.3 3D Stacked packages
 - 5.3.4 Fan-Out Wafer Level Packaging
 - 5.3.5 Flip Chip Package-on-Package
- 5.4 SiP Component Integration
- 5.5 Heterogeneous Integration Drivers
- 5.6 Trends Driving SiP Adoption
- 5.7 SiP Applications
- 5.8 SiP Industry Landscape
- 5.9 Future Outlook on Heterogeneous Integration

6 MONOLITHIC 3D IC

- 6.1 Overview
 - 6.1.1 Transitioning from 2D Systems
 - 6.1.2 Motivation for developing monolithic 3D manufacturing
 - 6.1.3 Improved M3D Interconnect Density
 - 6.1.4 Heterogenous 3D vs Monolithic 3D
 - 6.1.5 2D Materials
- 6.2 Benefits
- 6.3 Challenges

6.4 Future outlook

7 MARKETS AND APPLICATIONS

7.1 Market value chain

7.1.1 SiP OEM/Designers

7.1.2 Chiplet OEM/Designer and Chiplet Foundry

7.1.3 Chiplet Integrator

7.1.3.1 Integrated Device Manufacturers (IDMs)

7.1.3.2 Outsourced Semiconductor Assembly and Test (OSAT) Providers

7.1.4 Material Suppliers

7.1.5 Equipment Suppliers

7.1.6 Substrate and PCB suppliers

7.1.7 EDA Tools Suppliers

7.1.8 Interposer Foundry

7.2 Packaging trends by market

7.2.1 Mobile Devices

7.2.2 High-Performance Computing (HPC)

7.2.3 Automotive

7.2.4 Internet of Things (IoT)

7.2.5 Consumer Electronics

7.2.6 Aerospace and Defense

7.2.7 Medical Devices

7.3 Design requirements

7.4 Artificial Intelligence (AI)

7.4.1 Challenges in AI

7.4.2 Advanced Packaging Solutions

7.4.2.1 2.5D and 3D Integration

7.4.2.2 Chiplet-based Packaging

7.4.2.3 Wafer-Level Packaging (WLP)

7.4.3 Addressing AI Challenges through Advanced Packaging

7.4.3.1 Processing Power

7.4.3.2 Memory Bandwidth

7.4.3.3 Energy Efficiency

7.4.3.4 Scalability

7.4.4 Applications

7.4.4.1 Data Center and Cloud Computing

7.4.4.2 Edge Devices and IoT

7.4.4.3 Healthcare and Medical Devices

- 7.4.4.4 Autonomous Vehicles
- 7.5 Mobile Devices
 - 7.5.1 Challenges
 - 7.5.2 Advanced Packaging Solutions
 - 7.5.2.1 System-in-Package (SiP)
 - 7.5.2.2 Fan-Out Wafer-Level Packaging (FOWLP)
 - 7.5.2.3 3D IC Packaging
 - 7.5.2.4 Wafer-Level Chip-Scale Packaging (WLCSP)
 - 7.5.3 Addressing Challenges through Advanced Packaging
 - 7.5.3.1 Power Consumption and Thermal Management
 - 7.5.3.2 Size Constraints
 - 7.5.3.3 Cost
 - 7.5.4 Applications
 - 7.5.4.1 Smartphones
 - 7.5.4.2 Tablets
 - 7.5.4.3 Wearables
 - 7.5.4.4 AR/VR Devices
 - 7.5.5 Future trends
- 7.6 High Performance Computing (HPC)
 - 7.6.1 Challenges
 - 7.6.2 Advanced Packaging Solutions for HPC
 - 7.6.2.1 2.5D and 3D Integration
 - 7.6.2.2 Hybrid bonding
 - 7.6.2.3 Multi-Chip Modules (MCMs)
 - 7.6.2.4 Chiplet-based Architectures
 - 7.6.2.5 Advanced Interconnect Technologies
 - 7.6.3 Addressing HPC Challenges through Advanced Packaging
 - 7.6.3.1 Performance Scaling
 - 7.6.3.2 Power Consumption
 - 7.6.3.3 Interconnect Bandwidth
 - 7.6.3.4 Reliability
 - 7.6.4 Applications
 - 7.6.4.1 Supercomputers
 - 7.6.4.2 Data Center and Cloud Computing
 - 7.6.4.3 Artificial Intelligence and Machine Learning
 - 7.6.4.4 Scientific Computing and Simulation
 - 7.6.4.5 Co-Packaged Optics
 - 7.6.4.5.1 Network Switch
 - 7.6.4.5.2 Optical communication in data centers

- 7.6.4.5.3 Thermal Management
- 7.6.4.5.4 Challenges in CPO
- 7.6.4.5.5 Package Structure
- 7.6.4.5.6 Fan-Out Embedded Bridge (FOEB) structure
- 7.6.4.5.7 Advancing Switching and AI Networks
- 7.6.5 Future Trends
- 7.7 Automotive Electronics
 - 7.7.1 Challenges
 - 7.7.2 Advanced Packaging Solutions for Automotive Electronics
 - 7.7.2.1 System-in-Package (SiP)
 - 7.7.2.2 Flip-Chip and Wafer-Level Packaging (WLP)
 - 7.7.2.3 3D Integration and Through-Silicon Vias (TSVs)
 - 7.7.3 Addressing Automotive Electronics Challenges through Advanced Packaging
 - 7.7.3.1 ADAS/Autonomous driving systems
 - 7.7.3.2 Harsh Environment Reliability
 - 7.7.3.3 Safety and Reliability
 - 7.7.3.4 Miniaturization and Integration
 - 7.7.3.5 High-Speed Communication
 - 7.7.3.6 Thermal Management
 - 7.7.4 Applications
 - 7.7.4.1 Advanced Driver Assistance Systems (ADAS) and Autonomous Driving
 - 7.7.4.1.1 Radar packaging
 - 7.7.4.2 Electric Vehicle (EV) Power Electronics
 - 7.7.4.3 Infotainment and Telematics
 - 7.7.4.4 Sensors and Actuators
 - 7.7.5 Future Trends
- 7.8 Internet of Things (IoT) Devices
 - 7.8.1 Challenges
 - 7.8.2 Advanced Packaging Solutions for IoT Devices
 - 7.8.2.1 Wafer-Level Packaging (WLP)
 - 7.8.2.2 System-in-Package (SiP)
 - 7.8.2.3 Fan-Out Wafer-Level Packaging (FOWLP)
 - 7.8.2.4 3D Packaging and Through-Silicon Vias (TSVs)
 - 7.8.3 Addressing IoT Device Challenges through Advanced Packaging
 - 7.8.3.1 Size Constraints
 - 7.8.3.2 Power Consumption
 - 7.8.3.3 Cost Pressures
 - 7.8.3.4 Integration and Functionality
 - 7.8.3.5 Reliability and Robustness

- 7.8.4 Applications
 - 7.8.4.1 Wearable Devices
 - 7.8.4.2 Smart Home Devices
 - 7.8.4.3 Industrial IoT Devices
 - 7.8.4.4 Medical IoT Devices
- 7.8.5 Future Trends
- 7.9 5G & 6G Communications Infrastructure
 - 7.9.1 Challenges
 - 7.9.2 Trends in 5G and 6G packaging
 - 7.9.3 Advanced Packaging Solutions for 5G and 6G Communications Infrastructure
 - 7.9.3.1 Antenna-in-Package (AiP)
 - 7.9.3.2 System-in-Package (SiP)
 - 7.9.3.3 3D Packaging and Through-Silicon Vias (TSVs)
 - 7.9.3.4 Fan-Out Wafer-Level Packaging (FOWLP)
 - 7.9.4 Addressing 5G and 6G Infrastructure Challenges through Advanced Packaging
 - 7.9.4.1 High-Frequency Operation
 - 7.9.4.2 Massive MIMO and Beamforming
 - 7.9.4.3 Energy Efficiency
 - 7.9.4.4 Cost and Scalability
 - 7.9.4.5 Thermal Management
 - 7.9.5 Applications
 - 7.9.5.1 Base Stations and Small Cells
 - 7.9.5.2 Backhaul and Fronthaul Networks
 - 7.9.5.3 Edge Computing and Network Slicing
 - 7.9.5.4 Satellite and Non-Terrestrial Networks
 - 7.9.6 Future Trends
- 7.10 Aerospace and Defense Electronics
 - 7.10.1 Challenges
 - 7.10.2 Advanced Packaging Solutions for Aerospace and Defense Electronics
 - 7.10.2.1 3D Packaging and Through-Silicon Vias (TSVs)
 - 7.10.2.2 Chip-Scale Packaging (CSP) and Wafer-Level Packaging (WLP)
 - 7.10.2.3 Flip-Chip and Ball Grid Array (BGA) Packaging
 - 7.10.2.4 Hermetic Packaging and Sealing
 - 7.10.3 Addressing Aerospace and Defense Electronics Challenges through Advanced Packaging
 - 7.10.3.1 Size, Weight, and Power (SWaP) Optimization
 - 7.10.3.2 Harsh Environment Reliability
 - 7.10.3.3 High Performance and Speed
 - 7.10.3.4 Long-Term Reliability and Maintainability

- 7.10.3.5 Security and Anti-Tamper Features
- 7.10.4 Applications
 - 7.10.4.1 Avionics and Flight Control Systems
 - 7.10.4.2 Radar and Electronic Warfare Systems
 - 7.10.4.3 Satellite Communications and Payload Electronics
 - 7.10.4.4 Missile Guidance and Control Electronics
- 7.10.5 Future Trends
- 7.11 Medical Electronics
 - 7.11.1 Challenges
 - 7.11.2 Advanced Packaging Solutions for Medical Electronics
 - 7.11.2.1 3D Packaging and Through-Silicon Vias (TSVs)
 - 7.11.2.2 Wafer-Level Packaging (WLP) and Chip-Scale Packaging (CSP)
 - 7.11.2.3 Flexible and Stretchable Packaging
 - 7.11.2.4 Microfluidic Packaging
 - 7.11.3 Addressing Medical Electronics Challenges through Advanced Packaging
 - 7.11.3.1 Miniaturization
 - 7.11.3.2 Biocompatibility
 - 7.11.3.3 Reliability
 - 7.11.3.4 Power Efficiency
 - 7.11.3.5 High Performance
 - 7.11.4 Applications
 - 7.11.4.1 Implantable Devices
 - 7.11.4.2 Wearable Health Monitors
 - 7.11.4.3 Diagnostic Imaging Equipment
 - 7.11.4.4 Surgical Robotics and Instruments
 - 7.11.5 Future Trends
- 7.12 Consumer Electronics
 - 7.12.1 Challenges
 - 7.12.2 Advanced Packaging Solutions for Consumer Electronics
 - 7.12.2.1 System-in-Package (SiP)
 - 7.12.2.2 Fan-Out Wafer-Level Packaging (FOWLP)
 - 7.12.2.3 3D Packaging and Through-Silicon Vias (TSVs)
 - 7.12.2.4 Embedded Die Packaging
 - 7.12.3 Addressing Consumer Electronics Challenges through Advanced Packaging
 - 7.12.3.1 Miniaturization
 - 7.12.3.2 Power Efficiency
 - 7.12.3.3 High Performance
 - 7.12.3.4 Cost Reduction
 - 7.12.3.5 Time-to-Market

7.12.4 Applications

7.12.4.1 Smartphones and Tablets

7.12.4.2 Wearables and IoT Devices

7.12.4.3 Gaming Consoles and VR/AR Devices

7.12.4.4 Smart Home Devices

7.12.5 Future Trends

7.13 Additive manufacturing for advanced packaging

7.14 Silicon photonics

7.15 Global market (Revenues)

7.15.1 By type

7.15.2 By market

7.15.3 By region

8 MARKET PLAYERS

8.1 Integrated Device Manufacturers

8.2 Outsourced Semiconductor Assembly and Test (OSAT) Companies

8.3 Foundries

8.4 Electronics OEMs

8.5 Packaging Equipment and Materials Companies

9 MARKET CHALLENGES

10 COMPANY PROFILES

10.1 AaltoSemi

10.2 Absolic, Inc.

10.3 ACCRETECH (Europe) GmbH

10.4 Adeia, Inc.

10.5 Advanced Micro Devices, Inc. (AMD)

10.6 Analog Devices, Inc. (ADI)

10.7 Amkor Technology

10.8 Annuquan Intelligent Technology (AMQ Intelligent)

10.9 Apple

10.10 Applied Materials

10.11 Ardentec Corporation

10.12 ARM

10.13 ASE

10.14 ASMPT Ltd

- 10.15 Besi
- 10.16 Biren Technology
- 10.17 Blue Ocean Smart System
- 10.18 Brewer Science
- 10.19 Broadcom
- 10.20 BroadPak
- 10.21 Cambricon Technologies Co.,
- 10.22 Capcon Semiconductor
- 10.23 Casmeit
- 10.24 CAS Microelectronics Integration
- 10.25 CD Micro-Technology
- 10.26 CEA-Leti
- 10.27 Cerebras
- 10.28 China Wafer Level CSP Co
- 10.29 Chipbond Technology Corporation
- 10.30 Chipletz
- 10.31 ChipMOS Technologies, Inc.
- 10.32 Corning
- 10.33 Dewo Advanced Automation (DAA
- 10.34 Disco
- 10.35 Dupont
- 10.36 Ebara
- 10.37 Eliyan
- 10.38 EMC Semi-Conductor Technology
- 10.39 EPS Technology
- 10.40 Entegris
- 10.41 EV Group
- 10.42 GlobalFoundries
- 10.43 Global Unichip
- 10.44 Gloway
- 10.45 Goldenscope Tech
- 10.46 Gona Semiconductor Technology
- 10.47 Graphcore
- 10.48 Greatek Electronics Inc
- 10.49 Hangke Chuangxing (Aero Inno-Star)
- 10.50 Hanmi Semiconductor
- 10.51 HiSilicon
- 10.52 HLMC (Shanghai Huali Microelectronics Corporation)
- 10.53 Huatian Huichuang Technology (Xi'an) Co., Ltd.

- 10.54 Huawei
- 10.55 Ibsiden
- 10.56 IBM
- 10.57 ICLeague Technology Co Ltd
- 10.58 IMEC
- 10.59 Infineon Technologies AG
- 10.60 Integra
- 10.61 Inari Amertron Berhad
- 10.62 Intel Corporation
- 10.63 JCET Group
- 10.64 Jiangsu IC Assembly & Test (ICAT)
- 10.65 Jingdu Semiconductor
- 10.66 Keyang Semiconductor (KYS)
- 10.67 King Yuan Electronics Co., Ltd.
- 10.68 Kioxia
- 10.69 KyLitho
- 10.70 Kyocera
- 10.71 Lam Research
- 10.72 Lapis Technology
- 10.73 LB Semicon Co Ltd
- 10.74 Leading Interconnect Semiconductor Technology
- 10.75 Lidrotec GmbH
- 10.76 Lux Semiconductors
- 10.77 Malaysian Pacific Industries Berhad
- 10.78 Micron Technology, Inc.
- 10.79 Mediatek
- 10.80 Micross Components
- 10.81 Mitsubishi
- 10.82 National Center For Advanced Packaging China (NCAP China)
- 10.83 NEC
- 10.84 Nvidia Corporation
- 10.85 Nepes Corporation
- 10.86 Onsemi
- 10.87 Orient Semiconductor Electronics Ltd.
- 10.88 Panasonic
- 10.89 Powertech Technology Inc.
- 10.90 Pragmatic Semiconductor
- 10.91 Qorvo
- 10.92 Renesas

- 10.93 Rigger Micro Technologies (RMT)
- 10.94 Rohm
- 10.95 Rong Semiconductor
- 10.96 Samsung Electronics
- 10.97 Samtec, Inc.
- 10.98 Schott AG
- 10.99 Sharp
- 10.100 Shinko Electric Industries
- 10.101 Showa Denko
- 10.102 Sigurd Microelectronics Corporation
- 10.103 Silicon Box
- 10.104 Siliconware Precision Industries (SPIL)
- 10.105 SJ Semiconductor
- 10.106 SK Hynix
- 10.107 Skywater
- 10.108 Sony Corporation
- 10.109 Starmask
- 10.110 STMicroelectronics
- 10.111 Suss Microtec
- 10.112 SZLQ Intelligence (Suzhou Lieqi Intelligent Equipment)
- 10.113 Taiwan Semiconductor Manufacturing Company (TSMC)
- 10.114 Techsense International
- 10.115 Tezzaron Semiconductor
- 10.116 Tongfu Microelectronics Co., Ltd.
- 10.117 Texas Instruments
- 10.118 Tokyo Seimitsu Co., Ltd.
- 10.119 Tong Hsing Electronic Industries, Ltd.
- 10.120 Toshiba
- 10.121 Tower Semiconductor
- 10.122 Unimicron
- 10.123 Unisem
- 10.124 UTAC Group
- 10.125 Walton Advanced Engineering Inc.
- 10.126 Winstek Semiconductor Technology Co., Ltd.
- 10.127 Xinhe Semiconductor
- 10.128 Yibu Semiconductor
- 10.129 Yuehai Integrated

11 REFERENCES

List Of Tables

LIST OF TABLES

Table 1. Evolution of semiconductor packaging.

Table 2. Summary of key advanced semiconductor packaging approaches.

Table 3. Key Technology Trends in Advanced Semiconductor Packaging.

Table 4. Market Growth Drivers for advanced semiconductor packaging.

Table 5. Challenges Facing Advanced Packaging Adoption.

Table 6. Challenges in transistor scaling.

Table 7. Use cases and benefits of using chiplets in semiconductor design.

Table 8. Specifications of interconnection methods.

Table 9. Interconnection technique in semiconductor packaging

Table 10. Passive vs active interposer.

Table 11. Comparative benchmark overview table of key semiconductor interconnection technologies

Table 12. Fan-out packaging process overview.

Table 13. Comparison between mainstream silicon dioxide (SiO₂) and leading organic dielectrics for electronic interconnect substrates.

Table 14. Benefits of glass in 2.5D glass-based packaging.

Table 15. Comparison between key properties of glass and polymer molding compounds commonly used in semiconductor packaging applications.

Table 16. Challenges of glass semiconductor packaging.

Table 17. Comparison between silicon, organic laminates and glass as packaging substrates.

Table 18. 2.5D vs. 3D packaging.

Table 19. 2.5D packaging challenges.

Table 20. Market players in 2.5D packaging.

Table 21. Advantages and disadvantages of 3D packaging.

Table 22. Comparison between 2.5D, 3D micro bump, and 3D hybrid bonding.

Table 23. Challenges in 3D Hybrid Bonding.

Table 24. Challenges in scaling bumps.

Table 25. Key methods for enabling copper-to-copper (Cu-Cu) hybrid bonding in advanced semiconductor packaging:

Table 26. Micro bumps vs Cu-Cu bumpless hybrid bonding.

Table 27. Benefits of Wafer-Level Packaging.

Table 28. Types of wafer level packaging.

Table 29. Key trends shaping wafer level packaging.

Table 30. Packaging approaches utilized for assembling System-in-Package modules.

Table 31. Considerations for integrating key component categories into system-in-package (SiP) modules/

Table 32. Key factors driving adoption of heterogeneous integration through SiPs and multi-die packages.

Table 33. Key trends influencing adoption of System-in-Package modules.

Table 34. System-in-package (SiP) module applications.

Table 35. Comparison between heterogeneous 3D integration and monolithic 3D integration.

Table 36. Key 2D materials in monolithic 3D integrated circuits.

Table 37. Benefits of monolithic 3D ICs.

Table 38. Challenges of monolithic 3D ICs.

Table 39. Advanced semiconductor packaging trends by market.

Table 40. Design requirements in advanced packaging, by market.

Table 41. Global market for Advanced semiconductor packaging, 2020-2035, by packaging type, (billions USD).

Table 42. Global market for Advanced semiconductor packaging, 2020-2035, by end use market (billions USD).

Table 43. Recent expansion activities by companies in Malaysia.

Table 44. Global market for Advanced semiconductor packaging, 2020-2035, by region (billions USD).

Table 45 : Main Global Wafer Foundry Companies 2023.

Table 46. Market challenges for advanced semiconductor packaging.

Table 47. AMD AI chip range.

Table 48. Intel's products that adopt 3D FOVEROS.

List Of Figures

LIST OF FIGURES

- Figure 1. Timeline of different packaging technologies.
- Figure 2. Evolution roadmap for semiconductor packaging.
- Figure 3. Semiconductor Supply Chain.
- Figure 4. Advanced packaging supply chain.
- Figure 5. Scaling technology roadmap.
- Figure 6. Wafer-level chip scale packaging (WLCSP)
- Figure 7. Embedded wafer-level ball grid array (eWLB).
- Figure 8. Fan-out wafer-level packaging (FOWLP).
- Figure 9. Chiplet design.
- Figure 10. Chiplet SoC.
- Figure 11. 2D chip packaging.
- Figure 12. Typical structure of 2.5D IC package utilizing interposer.
- Figure 13. Fan-out chip-first process flow and Fan-out chip-last process flow.
- Figure 14. Manufacturing process for glass interposers.
- Figure 15. 3D Glass Panel Embedding (GPE) package.
- Figure 16. Typical FOWLP structure.
- Figure 17. System-in-Package (SiP) for HI.
- Figure 18. 2.5D chiplet integration.
- Figure 19. Advanced packaging supply chain.
- Figure 20. Packaging of sensors used in advanced driver assistance systems (ADAS) and autonomous driving.
- Figure 21. Global market for Advanced semiconductor packaging, 2020-2035, by packaging type, (billions USD).
- Figure 22. Global market for Advanced semiconductor packaging, 2020-2035, by end use market (billions USD).
- Figure 23. Global market for Advanced semiconductor packaging, 2020-2035, by region (billions USD).
- Figure 24. Absolic glass substrate.
- Figure 25. AMD Radeon Instinct.
- Figure 26. AMD Ryzen 7040.
- Figure 27. Alveo V70.
- Figure 28. Versal Adaptive SOC.
- Figure 29. AMD's MI300 chip.
- Figure 30. 12-layer HBM3.

I would like to order

Product name: The Global Market for Advanced Semiconductor Packaging 2024-2035

Product link: <https://marketpublishers.com/r/GD603A622464EN.html>

Price: US\$ 1,550.00 (Single User License / Electronic Delivery)

If you want to order Corporate License or Hard Copy, please, contact our Customer Service:

info@marketpublishers.com

Payment

To pay by Credit Card (Visa, MasterCard, American Express, PayPal), please, click button on product page <https://marketpublishers.com/r/GD603A622464EN.html>

To pay by Wire Transfer, please, fill in your contact details in the form below:

First name:
Last name:
Email:
Company:
Address:
City:
Zip code:
Country:
Tel:
Fax:
Your message:

****All fields are required**

Customer signature _____

Please, note that by ordering from marketpublishers.com you are agreeing to our Terms & Conditions at <https://marketpublishers.com/docs/terms.html>

To place an order via fax simply print this form, fill in the information below and fax the completed form to +44 20 7900 3970