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Global Fan Out Wafer Level Packaging Market Size Study, by Application (Analog and Mixed IC, Wireless Connectivity, Logic and Memory IC, MEMS and Sensors, CMOS Image Sensors) by Regional Forecasts 2017-2025

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Abstracts

Global Fan Out Wafer Level Packaging Market valued approximately USD xx billion in 2016 is anticipated to grow with a healthy growth rate of more than xx% over the forecast period 2017-2025 Increase in wafer size, the global semiconductor industry witnessed an increase in the size of silicon wafers, from 100 mm to 300 mm, which minimizes the cost of manufacturing semiconductor ICs by 20%-25%. At present, the industry predominantly uses 300 mm wafers to manufacturer ICs. This trend is expected to maintain its momentum during the forecast period as companies are investing a substantial amount in the construction and upgradation of fabs to manufacture 300 mm wafers. High adoption of semiconductor ICs in automobiles, the automation and electrification of automobiles has increased the need for semiconductor wafers. Several types of semiconductor ICs are used in automotive products such as GPS, airbag control, anti-lock braking system (ABS), power doors and windows, car navigation and display, infotainment, collision detection technology, and automated driving. This will propel the demand for WLP solutions for IC packaging in the automobile segment.

The objective of the study is to define market sizes of different segments & countries in recent years and to forecast the values to the coming eight years. The report is designed to incorporate both qualitative and quantitative aspects of the industry within each of the regions and countries involved in the study. Furthermore, the report also caters the detailed information about the crucial aspects such as driving factors & challenges which will define the future growth of the market. Additionally, the report shall also incorporate available opportunities in micro markets for stakeholders to invest

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along with the detailed analysis of competitive landscape and product offerings of key players. The detailed segments and sub-segment of the market are explained below:

By Application:

Analog and mixed IC

Wireless connectivity

Logic and memory IC

MEMS and sensors

CMOS image sensors

By Regions:

North America

U.S.

Canada

Europe

UK

Germany

Asia Pacific

China

India

Japan

Latin America

Brazil

Mexico

Rest of the World

Furthermore, years considered for the study are as follows:

Historical year – 2015
Base year – 2016
Forecast period – 2017 to 2025

Some of the key manufacturers involved in the market are STATS Chip PAC, TSMC, Texas Instruments, SEMES, Rudolph Technologies, SUSS Micro Tec., Acquisitions and effective mergers are some of the strategies adopted by the key manufacturers. New product launches and continuous technological innovations are the key strategies adopted by the major players.

Target Audience of the Global Fan Out Wafer Level Packaging Market in Market Study:

Key Consulting Companies & Advisors

Large, medium-sized, and small enterprises

Venture capitalists

Value-Added Resellers (VARs)

Third-party knowledge providers

Investment bankers

Investors

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