Global 3D IC and 2.5D IC Packaging Market Size Study & Forecast, by Packaging Technology (3D Wafer-Level Chip Scale Packaging, 3D TSV and 2.5D), Application (Logic, Memory, MEMS/Sensors, Imaging & Optoelectronics, LED), and Regional Forecasts 2025–2035

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Abstracts

The Global 3D IC and 2.5D IC Packaging Market is valued approximately at USD 60.41 billion in 2024 and is projected to expand at a CAGR of 10.70% over the forecast period 2025–2035. 3D IC and 2.5D IC packaging technologies represent the forefront of semiconductor integration, allowing multiple dies to be stacked or interconnected in a single package, thereby drastically enhancing performance, reducing form factor, and improving power efficiency. These packaging solutions are increasingly pivotal in driving the miniaturization of advanced electronic devices and enabling next-generation computing, AI accelerators, and high-bandwidth memory solutions. The growth of the market is fueled by the surging demand for high-performance computing, mobile devices, and data center solutions, alongside the ongoing evolution of heterogeneous integration techniques and advanced interconnect architectures. Moreover, manufacturers are investing heavily in R&D to optimize thermal management, signal integrity, and reliability within stacked and interposer-based packages.

The rising adoption of high-performance devices and emerging technologies such as artificial intelligence, machine learning, and IoT has catalyzed the demand for 3D and 2.5D packaging. These advanced packaging techniques address challenges posed by traditional 2D packaging limitations, offering higher I/O density, reduced latency, and improved electrical and thermal characteristics. According to market insights, the deployment of 3D TSV and 2.5D interposers has become critical in enabling high-

bandwidth memory stacks, graphics processing units, and complex SoC architectures. While the market enjoys robust growth prospects, it is also influenced by high manufacturing costs, technical complexities, and evolving fabrication capabilities. Nevertheless, as semiconductor companies increasingly prioritize miniaturization, enhanced device performance, and energy efficiency, the market for 3D IC and 2.5D IC packaging is set to witness substantial expansion through 2035.

The detailed segments and sub-segments included in the report are:

By Packaging Technology:

- 3D Wafer-Level Chip Scale Packaging
- 3D TSV and 2.5D

By Application:

- Logic
- Memory
- MEMS/Sensors
- Imaging & Optoelectronics
- LED

By End User:

- Consumer Electronics
- Automotive
- Telecom & IT
- Industrial & Manufacturing

- Healthcare & Medical Devices
- Others

By Region:

North America

- U.S.
- Canada

Europe

- UK
- Germany
- France
- Italy
- Spain
- Rest of Europe

Asia Pacific

- China
- Japan
- South Korea
- India

  - Taiwan
  - Rest of Asia Pacific

- Latin America
  - Brazil
  - Mexico

- Middle East & Africa
  - UAE
  - Saudi Arabia
  - South Africa
  - Rest of Middle East & Africa

Among the various applications, logic devices are expected to dominate the market due to the growing demand for high-performance computing and mobile processing solutions. Logic ICs benefit greatly from 3D and 2.5D packaging, which enables stacking of processor cores and high-speed memory in compact footprints, significantly improving computational efficiency and power performance. Moreover, the expansion of AI, HPC, and cloud computing infrastructures continues to drive the adoption of advanced packaging solutions in logic applications. While logic remains the market leader in revenue share, memory applications—particularly high-bandwidth memory and next-generation DRAM—are rapidly gaining traction as manufacturers seek enhanced bandwidth, reduced latency, and improved thermal performance in stacked configurations.

When segmented by packaging technology, 3D TSV and 2.5D packaging currently lead the revenue contribution, owing to their ability to deliver higher integration density and superior electrical performance for complex semiconductor architectures. These technologies are increasingly deployed in data centers, GPUs, AI accelerators, and other high-performance devices. Meanwhile, 3D wafer-level chip scale packaging offers advantages in miniaturization and cost efficiency, making it particularly attractive for mobile devices and consumer electronics. The coexistence of these technologies illustrates a nuanced market landscape: 3D TSV/2.5D dominates in performance-intensive segments, while wafer-level chip scale packaging provides optimized solutions for size- and cost-sensitive applications.

The key regions considered for the Global 3D IC and 2.5D IC Packaging Market study include Asia Pacific, North America, Europe, Latin America, and the Middle East & Africa. North America held the largest market share in 2025 due to its established semiconductor ecosystem, strong presence of leading foundries, and early adoption of advanced packaging technologies. Asia Pacific is anticipated to be the fastest-growing region over the forecast period, driven by aggressive semiconductor manufacturing expansion in China, Taiwan, Japan, and South Korea. These countries are investing in advanced packaging infrastructure, driven by demand from consumer electronics, automotive electronics, and industrial automation sectors. Europe maintains a stable growth trajectory with its focus on automotive, telecom, and industrial IoT applications, whereas Latin America and the Middle East & Africa are gradually increasing their adoption, primarily influenced by emerging electronics manufacturing and technological modernization initiatives.

Major market players included in this report are:

- ASE Technology Holding Co., Ltd.
- TSMC Limited
- Intel Corporation
- Samsung Electronics Co., Ltd.
- Amkor Technology, Inc.
- STATS ChipPAC Ltd.
- JCET Group Co., Ltd.
- Powertech Technology Inc.

- SPIL (Siliconware Precision Industries Co., Ltd.)
- UTAC Holdings Ltd.
- Silicon Works Co., Ltd.
- J-Devices Corporation
- Advanced Semiconductor Engineering (ASE)
- Intel Foundry Services
- Texas Instruments Incorporated

Global 3D IC and 2.5D IC Packaging Market Report Scope:

- Historical Data – 2023, 2024
- Base Year for Estimation – 2024
- Forecast period – 2025–2035
- Report Coverage – Revenue forecast, Company Ranking, Competitive Landscape, Growth factors, and Trends
- Regional Scope – North America; Europe; Asia Pacific; Latin America; Middle East & Africa
- Customization Scope – Free report customization (equivalent to up to 8 analysts' working hours) with purchase. Addition or alteration to country, regional & segment scope*

The objective of the study is to define market sizes of different segments and countries in recent years and to forecast the values for the coming years. The report is designed to incorporate both qualitative and quantitative aspects of the industry within the countries involved in the study. The report also provides detailed information about crucial aspects, such as driving factors and challenges, which will define the future growth of the market. Additionally, it incorporates potential opportunities in micro-markets for stakeholders to invest, along with a detailed analysis of the competitive landscape and product offerings of key players. The detailed segments and sub-segments of the market are explained below:

Key Takeaways:

- Market Estimates & Forecast for 10 years from 2025 to 2035.
- Annualized revenues and regional-level analysis for each market segment.
- Detailed analysis of the geographical landscape with country-level analysis of major regions.
- Competitive landscape with information on major players in the market.
- Analysis of key business strategies and recommendations on future market approach.
- Analysis of the competitive structure of the market.
- Demand side and supply side analysis of the market.

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